Inelastic electron tunneling spectroscopy study of traps in ultrathin high-

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We report the use of inelastic electron tunneling spectroscopy (IETS) as an effective tool in studying traps in high-

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This letter will shed some lights on the nature of these two kinds of traps, which are not available from conventional measurements. Particular attention is paid to the electrical stress-induced traps.

Figure 1 illustrates the basic difference between the aforementioned trap effects in $I-V$ and $d^2I/dV^2-V$ plots. Curve (1) in Fig. 1(a) shows that the $I-V$ curve will show an increase in slope over a small range of voltage when trap-assisted conduction mechanism takes place, where the voltage at which this occurs corresponds to the trap energy (in electron-volt) above the Fermi level in equilibrium, and the width of this region corresponds to the energy spread of this particular trap, including thermal spread. Curve (2) in Fig. 1(a) shows that charge trapping effect causes a small horizontal plateau, where the width of the plateau is proportional to the trapped charge ($\Delta V=qN_t/C_{ox}$, where $q$ is the electron charge, $N_t$ is the areal trap density, and $C_{ox}$ is the gate

FIG. 1. Illustration of two kinds of trap effects on (a) $I-V$ and (b) $d^2I/dV^2-V$ characteristics. In each case, curve (1) represents trap-assisted conduction and curve (2) represents carrier trapping.
dielectric capacitance). Note that this effect is analogous to the well-known capacitance–voltage shift due to charge trapping. Figure 1(b) shows the corresponding second derivative of the $I$–$V$ curve; specifically, the second derivative will show a peak-followed-by-a-valley for the trap-assisted conduction mechanism (curve 1), while a valley-followed-by-a-peak for the charge trapping mechanism (curve 2).

The MOS capacitors in this study were fabricated on $n$-type, (100) silicon substrates. Degenerate silicon wafers were used to ensure conduction at the liquid He temperature (4.2 K) used for the IETS measurement to ensure that the Si substrate remains highly conductive at cryogenic temperatures, which behaves very much like a metal. It is worth noting that, because of the metallic behavior of the degenerate silicon substrate with very small resistance, there is very little voltage drop across it during the IETS measurement, and thus the applied voltage can be considered to be completely dropped across the gate dielectric, regardless of the charge in the gate dielectric or at the interface.

The HfO$_2$ layers under investigation were deposited by the jet vapor deposition (JVD) technique at room temperature. The as-deposited physical thickness of each dielectric film was about 2 nm, estimated from the deposition rate of the JVD system. A postdeposition anneal was performed in N$_2$ at 600 °C for 5 min. Aluminum, approximately 300 nm thick, was deposited as top electrode by thermal evaporation for all samples. The size of each MOS capacitor was 1 mm$^2$ in area. Each IETS spectrum ($d^2I/dV^2$ vs $V$ plot) was measured at liquid helium temperature (4.2 K) with the standard lock-in method.

Figure 2 shows the room temperature current–voltage curves of an Al–HfO$_2$–Si capacitor before and after a series of constant-voltage stresses at 1.2 V at room temperature. It is apparent that the current increases noticeably as the stressing time increases. This is the stress-induced-leakage current that is often observed for ultrathin gate dielectrics, and is believed to be related to the buildup of traps in the gate dielectric.

Figure 3 shows the corresponding IETS spectra of the device discussed earlier, where curve (a) was taken before the stress, and the most prominent peak at 58 mV corresponds to Si phonon vibration; other features are relatively weak, but if sufficiently amplified we could identify possible Hf–O vibrations at about 34, 48, and 70 mV, Hf–O–Si and Si–O vibration modes from 130 to 160 mV, and possible hydrogen bonds related vibration modes at about 110 and 255 mV. Curve (b) in Fig. 3 was taken after constant-voltage stress at 1.2 V for 200 s. Many additional features appear between 130 and 300 mV, indicating electrical stress-induced buildup of defects. Curve (c) in Fig. 3 was taken after constant-voltage stress for 800 s, and one can see a dramatic increase in magnitude of the features between 160 and 200 mV, and between 250 and 290 mV. It seems that both kinds of trap effects as depicted in Fig. 1 are found in curve (c), where the feature marked (1) may be attributed to trap-assisted conduction, the feature marked (2) may be associated to trapping, while that marked (3) may also be associated with trapping. Similarly, the features between 250 and 290 mV also appear to contain both kinds of traps.

The fact that a group of major trap-related features appears between 160 and 200 mV suggests that they may be associated with some characteristic bonding defects with energies reachable by an applied voltage of around 180±20 meV. Similarly, the group of features appearing between 250 and 290 meV suggests that some electrically active defects have energies reachable by an applied voltage of around 270±20 mV. It will be an interesting challenge to identify such characteristic defects either by other spectroscopic methods or by theoretical calculation. Another useful piece of information from the data of curve (c) in Fig. 3 is that both trap-assisted conduction mechanism and trapping effect occur with a small energy separation within each group, which may indicate that they originate from very similar kind of defects, but perhaps with slight differences in their surrounding environments.

In addition to the two groups of features discussed earlier, there are also other, smaller, features on curve (c) in Fig. 3 as a result of electrical stress, and they can be attributed to traps as well.

Figure 4 shows the IETS spectra taken with two different voltage polarities. The upper half of Fig. 4 depicts the spectra taken with a forward bias (i.e., with the gate electrode biased positively with respect to the $n$-type Si substrate), while the lower half depicts the spectra taken under a reverse bias. It has been shown that the upper half of the spectra in Fig. 4...
positive electrode, and therefore they will see a higher tunnel barrier throughout much of the journey to the anode, which causes the IETS signal to be smaller. On the other hand, if the tunneling electrons traverse the tunnel barrier without losing energy until they arrive near the anode where they undergo inelastic interactions to lose some energy, then these electrons see a lower barrier throughout much of the journey to the anode, which results in a higher IETS signal relative to the former case. Based on this asymmetric polarity dependence, one can thus use IETS to probe inelastic features near either one interface or the other by switching the polarity of the voltage bias.

It should be noted that the previous paragraph does not apply to the trap features that we have discussed, either those associated with trap-assisted tunneling or those associated with electron trapping, as these processes are basically elastic. The location of a trap, however, can be determined by its forward and reverse IETS spectra, as will be shown in a future publication.

Before the electrical stress, one can see that the major features for both polarities are associated with Si phonons, Si–Hf–O and Si–O bonds, as expected. The Al–O feature, arising from the gate electrode, appears to be present as well. There also appears to be some trap-related features in between these major features. After the electrical stress, one can see at least three features that can be ascribed to traps: two in the forward-biased spectrum. The microscopic origins of these traps and their evolution as a function of time remain to be studied.

In summary, we have applied the IETS technique to study electrically-active traps in MOS capacitors with ultrathin HfO₂ as the gate dielectric. It has been shown that the IETS technique enables the identification of two different kinds of trap effects, that of carrier trapping and that of trap-assisted conduction. The IETS technique also allows the determination of the energy level as well as its spatial location (to some extent) of a trap. These capabilities are very useful for studying the microscopic origins of these traps, which are not available with conventional techniques.

In addition to results reported in this letter, we have applied IETS to MOS capacitors with HfO₂ gate prepared under various process conditions, as well as MOS capacitors with thermal SiO₂ as the gate dielectric. We found that MOS capacitors with thermal SiO₂ as the gate dielectrics have significantly fewer trap-related features, and it also requires much higher stress voltages (about 3 V) to generate the trap related defects. We have also found that IETS of HfO₂ capacitors produced under different process conditions exhibit similar trap related features. Further investigation is currently underway to study the energy levels and spatial distributions of the dominant trap related defects in high-k gate dielectrics, and their relation to dielectric breakdown.

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