The Impact of Device Scaling on the Current Fluctuations in MOSFET’s
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Abstract—The impact of device scaling on modern MOS technology is discussed in terms of the random telegraph signals and 1/f noise in MOSFET’s. In addition to the more obvious effects of enhanced current fluctuations as the device is scaled down, we will show the influence of nonuniform distribution of threshold voltages along the channel in the context of device scaling. The role of fast interface states on the drain current fluctuations will also be discussed. It will be shown that, compared to the oxide traps, fast interface states give rise to higher-frequency RTS and 1/f noise, and that they become more important for devices operating in weak inversion.

I. INTRODUCTION

As the device dimensions continue to shrink with each new generation of MOS technology, the effect of an individual defect on device performance becomes more pronounced. In MOSFET’s with submicron channel lengths and widths, the so-called random telegraph signals (RTS’s), characterized by discrete switching events of the channel current, have often been observed and attributed to the trapping/detrapping of conduction carriers by individual interfacial defects [1], [2]. Since the 1/f noise, which has been extensively studied for decades [1]–[7], is widely recognized as resulting from the superposition of numerous RTS events [1], [2], [5], [7], the studies of RTS’s have contributed greatly to our understanding of the nature of 1/f noise in MOSFET’s.

The purpose of this paper is to bring out some device down-scaling issues relating to the aforementioned current fluctuations in MOSFET’s. We will first verify that both the amplitude of RTS’s and the 1/f noise increase as the channel length decreases [3], [4]. A simple theory will be presented which shows that, for a given surface potential and fixed drain voltage, the RTS amplitude is a quadratic function of 1/L, where L is the effective channel length, while the 1/f noise power density is proportional to 1/L^3. By the use of a special test device structure, we will demonstrate quantitatively good agreement between our experimental results and the simple theory. Using this as a basis, we will show that nonuniform distribution of threshold voltages along the channel will cause an enhanced current fluctuation. This threshold nonuniformity could arise either from laterally nonuniform distribution of the dopant concentration or hot-carrier induced charge trapping near the drain junction; both are more likely to happen for MOSFET’s with shorter channels.

We will then discuss the effects of fast interface states. By fast interface states, we mean the D_{it} or N_{it} as measured by the standard techniques, such as capacitance or conductance measurements on MOS capacitors and charge pumping or subthreshold slope measurements on MOSFET’s, regardless of their physical origins. In the past, most of the work on RTS’s and 1/f noise in MOSFET’s published in the literature had focused on the effects of oxide traps near the interface [1], [2], [8], but little attention had been paid to those of fast interface states, despite their well-known ability to trap carriers and their well-documented effects on device performance. In the last section of this paper, we will demonstrate that fast interface states do give rise to current fluctuations, although the frequencies of these fluctuations are generally higher than those caused by oxide traps.

Accompanying the dimensional scaling in modern MOS technology is the reduction of the operating voltages to improve the device reliability and to avoid excessive power consumption. As a consequence, the subthreshold characteristics of MOSFET’s become ever more important. It will be shown that the contribution of the fast interface states to the current fluctuations is also more enhanced in the subthreshold regime. Furthermore, this contribution is even greater for devices that have a nonuniform distribution of threshold voltages.

II. BRIEF DESCRIPTION OF RANDOM TELEGRAPH SIGNALS AND 1/f NOISE IN MOSFET’S

The RTS’s in a MOSFET, characterized by discrete drain current fluctuations, is believed to be due to the trapping/detrapping events caused by an individual interface defect near Si/SiO2 interface [1], [2], [8]. Fig. 1 shows an example of the RTS trace for an n-channel MOSFET, where three key parameters are marked on the RTS trace: the capture time τ_c, the emission time τ_e, and the current fluctuation amplitude ΔI_d. For an n-channel device, τ_c is the average time at the high current state, τ_e is the average time at the low current state, and ΔI_d is the discrete switching amplitude caused by the combined effect of a change in the number of conduction carriers due to trapping/detrapping events and a local mobility modulation due to the trapped charge [2], [5], [11].

The 1/f noise can be viewed as a superposition of all the electrically active RTS’s [1], [2], [5], [7]. Therefore, both the fluctuations of the carrier density due to trapping/detrapping

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and the resulting changes of the carrier mobility will contribute to the 1/f noise.

Our experimental setup for measuring the RTS's and the 1/f noise power spectrum of the drain current fluctuations has been described elsewhere [12]. A current amplifier is used to supply a fixed drain bias (0.1 V) as well as to amplify the current fluctuations. The adjustable current suppression function in the current amplifier allows us to preset the bias drain current instead of the gate voltage. An HP3561 signal analyzer with a frequency range from 10 Hz to 100 kHz is used to sample the data and to perform the Fourier transformation. Time domain data (for RTS analysis) and frequency domain data (for 1/f noise analysis) can be stored simultaneously in a data file. Typically, more than 100 switching events of RTS's and more than 40 repetitions of frequency spectrum data are taken and averaged in order to obtain statistically accurate results.

III. CHANNEL LENGTH DEPENDENCE OF RTS

A. Theory

For a small drain voltage \( V_d \), the drain current \( I_d \) of a MOSFET can be expressed as

\[
I_d = (W/L) \mu Q_s V_d
\]

where \( W \) is the channel width, \( L \) is the channel length, \( \mu \) is the carrier mobility, and \( Q_s \) is the areal charge density of the conducting carriers in the channel. The current fluctuation due to a trapping/detrapping event can then be written from (1) as

\[
\Delta I_d = (W/L)(\mu \Delta Q_s + Q_s \Delta \mu)V_d.
\]

In this equation, the first term in the second bracket on the right hand side arises from the change of the number of carriers in the channel, while the second term comes from the mobility modulation effect due to the change in the trapped charge.

Now we will proceed to estimate the amplitude of the RTS in the context of device scaling.

Defining \( Q_s = qN/(WL) \), where \( N \) is the total number of carriers without trapping events in the channel, and \( \Delta Q_s = q/(WL) \) (assuming trapping/detrapping of a single carrier), we have

\[
\Delta I_d = (1/L^2) q \mu V_d + (W/L) Q_s (\Delta \mu)V_d.
\]

The first term on the right hand side of this equation suggests that, if one measures RTS's at a fixed average carrier density of \( Q_s \), \( \Delta I_d \) could scale inversely with \( L^2 \), while the second term on the right hand side suggests a linear dependence on \( 1/L \). In the case where the mobility fluctuation is negligible, then (3) can be approximated by

\[
\Delta I_d = (1/L^2) q \mu V_d.
\]

B. Experimental Verification

The n-channel MOSFET's used in this study have oxide thickness of 115 Å and drawn channel width of 1.2 μm. The drawn channel length ranges from 1.3 μm down to 0.7 μm. \( \Delta W/\Delta L \) are determined to be 0.6/0.35 μm. For clarity of the text, the effective channel length and the effective channel width are expressed as \( L \) and \( W \), respectively.

The special test structure for determining the channel length dependence of the current fluctuation is shown in Fig. 2, where all MOSFET's have the same channel width with various channel lengths. These MOSFET's all share a common gate, and therefore have the same surface potential during the noise measurement. By keeping the same grounded source and moving the drain terminal from \( D_1 \) to \( D_2 \), one can increase the channel length from \( L_1 \) to \( L_1 + L_2 \). Similarly, one can successively increase the channel length by moving the drain terminal to \( D_3, D_4, \) etc. A constant drain voltage of 0.1 V is applied to the drain during the RTS measurement.

To examine the channel length dependence of the RTS amplitude qualitatively, we first measured the RTS signals on a set of devices within the same chip with three different channel lengths. Fig. 3 shows a compilation of the RTS amplitude
data as a function of the normalized drain current \(\frac{L/W}{I_d}\) for these devices. This variable is chosen here because it is proportional to the channel carrier density. The three dotted lines are aids to the eye.

Even though there is large scattering in the data, the qualitative trend is unmistakable; i.e., for a given normalized drain current (or surface potential), the RTS amplitude tends to increase with a shorter channel length. However, it is impossible to extract quantitatively the channel length dependence from such data.

The scattering in the data comes from the fact that numerous different defects are included in this plot. Since the RTS amplitude not only depends on the channel length, but also depends on the nature of the defect (such as its location and energy), it is not surprising that we would see large scattering in a plot such as the one in Fig. 3.

To avoid this complication arising from numerous defects, we designed an experiment based on the special test structure shown in Fig. 2, which allows us to study the channel length dependence of the RTS amplitude associated with only one defect. The channel length may be varied over a wide range by selecting different drain terminals, from \(D_1\) to \(D_n\), with a common grounded source.

To begin with, we first find a prominent RTS signal in the shortest device (Device 1) by placing the drain voltage at terminal \(D_1\), and record its amplitude and background drain current. Without changing the common-gate voltage, we then progressively increase the effective channel length by adding Device 2, Device 3, \ldots, \ldots, in series, and measure the RTS amplitude arising from the same defect. The RTS signal from a given defect is characterized by its average capture time and emission time, and thus can be easily identified and tracked. Since we are tracking the RTS due to the same defect in Device 1, the change in the RTS amplitude as we add more devices in series can only be due to the increased channel length.

Fig. 4(a) shows the RTS amplitude arising from one defect as a function of the inverse channel length. Since the measurement was performed at a given surface potential, the background drain current (marked on the top scale) is proportional to the inverse channel length. The data in Fig. 4(a) clearly indicate a superlinear dependence of the RTS amplitude on the inverse channel length. When we plot the square root of the RTS amplitude, a nearly linear dependence of the inverse channel length is obtained, as shown in Fig. 4(b). This is consistent with the theoretical prediction of (4).

Note that (3) suggests that, in general, the drain current fluctuation is a combined effect of carrier number fluctuation (1st term on the right hand side) and mobility fluctuation (2nd term on the right hand side). In the case where the number fluctuation effect dominates, the RTS amplitude should be proportional to \(1/L^2\); while in the case where the mobility fluctuation effect dominates, the RTS amplitude should be proportional to \(1/L\). Our data in Fig. 4 indicate that, for this particular RTS, the dominant contribution is from the carrier number fluctuation due to trapping/detrapping of a single electron.

Since in (3) the mobility fluctuation term is proportional to \(W/L\), which tends to stay constant as one scales down the device dimensions (i.e., both \(W \) and \(L \) tend to scale down by the same factor), one would expect the number fluctuation term to dominate as the device gets smaller. The fact that
this term increases quadratically with $1/L$ raises concern for future deep submicron MOSFET’s.

IV. CHANNEL LENGTH DEPENDENCE OF $1/f$ NOISE

A. Theory

It has been shown [7] that the power density of the drain current noise in a MOSFET, $S_{I_d}(f)$, may be expressed as

$$S_{I_d}(f) = \frac{kT\gamma}{\gamma TL^2} \left( \frac{1}{N} + \alpha \mu \right)^2 N_i(E_{Fn})$$  \hspace{1cm} (5)

where $k$ is the Boltzmann constant, $T$ is the absolute temperature, $\gamma$ is the attenuation coefficient of the electron wavefunction in the oxide, $f$ is the frequency of the noise spectrum, $N$ is the carrier density per unit area, $\alpha$ is the scattering coefficient associated with the trapped charge, $N_i$ is the occupied trap density per unit area, and $E_{Fn}$ is the quasi Fermi level.

It should be noted that the following assumptions [7] have been made in arriving at (5)

1) the interfacial traps have a uniform areal distribution throughout the gate area;
2) the trapping time constant increases exponentially with the distance of the oxide trap from the interface; and
3) the drain voltage is sufficient low such that the carrier density is uniform along the channel.

Substituting the drain current in (1) into (5), we have

$$S_{I_d}(f) = \frac{kT\gamma}{\gamma TL^2} (\mu V_d)^2 (q + Q_o \alpha \mu)^2 N_i(E_{Fn})$$ \hspace{1cm} (6)

This equation indicates that, when everything else is held constant, the noise power density of the drain current is proportional to $1/L^3$.

B. Experimental Verification

The special test structure shown in Fig. 2 is again used in this experiment. To make the measurement easier and to reduce the ambiguity of the data, we deliberately increase the $1/f$ noise of the MOSFET’s by subjecting them to a positive Fowler–Nordheim (FN) electron injection at $V_d = 10$ V, and $V_d = V_s = V_{sub} = 0.0$ V for 1000 s.

Fig. 5 shows the noise power spectra of the drain current measured after FN injection at four different drain terminals (i.e., $D_1$–$D_4$) under a fixed gate voltage of 0.75 V and a fixed drain voltage of 0.1 V. The corresponding effective channel length is marked for each curve. The data clearly indicate that the noise power density increases over the entire frequency range as the effective channel length decreases.

To determine the channel length dependence of the noise power density more quantitatively, we plot the power densities as functions of the effective channel length for the data measured at 10 Hz, 100 Hz, 1 kHz, and 10 kHz, respectively. The dashed line corresponds to the theoretical fit to the $1/L^3$ dependence. One can see that the actual dependence is somewhat stronger than $1/L^3$ in the submicron regime. The discrepancy between the experimental data and theory may be due to the errors in estimating the effective channel lengths and nonuniform distribution of the interfacial defects.

In fact, we have strong evidence to show that a nonuniform distribution of the charged interfacial defects could cause a significant increase of the $1/f$ noise spectrum in a MOSFET. The effect of channel nonuniformity will be discussed in the next section.

These results suggest that the drain current noise increases much faster than the device downscaling factor. As indicated in (6), even if one scales down the channel width $W$ together with the channel length $L$ such that the $W/L$ ratio stays unchanged, the drain current noise would still increase by a factor of $1/L^2$. This raises concern about the performance of future generations of deep-submicron MOSFET’s for certain applications where low drain current noise is required.

V. EFFECTS OF NONUNIFORM DISTRIBUTION OF THRESHOLD VOLTAGES

A. Theory

The effects of channel nonuniformity can be understood by first considering a MOSFET which has two regions of different threshold voltages. The derivation can then be extended to include more than two electrically distinct regions.

The two-region MOSFET is often encountered in practice. For example, the region near the source/drain could have a different threshold voltage than the bulk of the channel due to the different doping concentrations. Another example could be a higher threshold voltage near the drain than the bulk of the channel due to electron trapping after channel-hot-electron stress.

The drain voltage and the corresponding noise power for a two-region MOSFET can be modeled as [13]

$$V_d = V_1 + V_2$$  \hspace{1cm} (7)

and

$$S_{I_d}(f) = S_{V_1}(f) + S_{V_2}(f)$$ \hspace{1cm} (8)
where subscripts 1 and 2 denote the two transistor regions. Suppose one region, say region 1, has a higher threshold voltage, and the other region, say region 2, has a lower threshold voltage. Converting the voltage fluctuations in (8) into current fluctuations, we have

\[ S_{I_d}(f) = \frac{S_{I_1}(f)}{G_1^2} + \frac{S_{I_2}(f)}{G_2^2}. \]  

(9)

Here, \( G_i = \mu_i Q_i W_i / L_i \) (\( i = 1, 2 \)) is the channel conductance associated with region \( i \); \( G = (G_1^{-1} + G_2^{-1})^{-1} \) is the total current conductance, and \( I_d = I_1 = I_2 \) is the drain current.

To see more clearly the contributions of the two regions, we express \( S_{I_1} \) and \( S_{I_2} \) in terms of (6). Substituting (1) for \( I_d \):

\[ S_{I_1}(f) = \frac{kT W}{\xi_f L_1^2} (\mu_1 V_1^2)(q + Q_{11} \alpha \mu_1)^2 N_{11}(E_{F1}) \]  

(10)

\[ S_{I_2}(f) = \frac{kT W}{\xi_f L_2^2} (\mu_2 V_2^2)(q + Q_{22} \alpha \mu_2)^2 N_{22}(E_{F2}) \]  

(11)

and taking into consideration that \( V_i = V_d G_i^{-1} / (G_1^{-1} + G_2^{-1}) \), we can rewrite (9) as

\[ S_{I_d}(f) = \frac{kT W}{\xi_f L_1^2} (\mu_1 V_d^2)^2 \left[ (\mu_1 Q_{11} \alpha \mu_1)^2 N_{11}(E_{F1}) \right. \
\left. + (\mu_2 Q_{22} \alpha \mu_2)^2 N_{22}(E_{F2}) \right] \]  

(12)

where the first term in the bracket represents the noise from region 1, and the second term from region 2.

Because of the higher threshold voltage in region 1 than in region 2, under a given gate bias \( Q_{11} \) can be very much smaller than \( Q_{22} \). In the case that \( Q_{22} / Q_{11} \gg Q_{11} / L_1 \), the noise from region 1 will dominate, and (12) can be reduced to

\[ S_{I_d}(f) = \frac{kT W}{\xi_f L_1^2} (\mu_1 V_d)^2 (q + Q_{11} \alpha \mu_1)^2 N_{11}(E_{F1}). \]  

(13)

When compared to the case for the uniform channel where the noise is expressed as (6), (13) represents a factor of \( (L_1 / L_2)^3 \) increase. The net result could be a dramatically enhanced drain current fluctuation due to a small region \( (L_1) \) of higher threshold voltages than the rest of the channel.

It should be noted that the theory presented above is highly simplified. Nonetheless, it serves to illustrate the main point of this paper; i.e., the nonuniform distribution of the threshold voltages along the channel could cause a significant increase of the 1/f noise.

B. Experimental Verification

The n-channel MOSFET’s used in this study have an oxide thickness of 250 Å with a channel length of 10 μm and a channel width of 25 μm. Relatively long channel devices are used to accentuate the effect of channel nonuniformity on the 1/f noise.

The channel \( V_{th} \) nonuniformity is created by a negative-gate Fowler–Nordheim (FN) injection (at \( V_g = -23.5 \) V for 100 s, with all other terminals grounded) that is known to cause a more positive (or less negative) threshold voltage shift near the source and the drain junctions than that in the main channel for this set of devices [14]. This is due to enhanced electron trapping near the channel edges [14].

In some of the FN damaged devices, a local hot-hole injection scheme is subsequently used to neutralize the trapped electrons near the channel edges so as to bring down the local threshold voltages in these regions. To inject holes near the drain junction, the bias conditions are \( V_g = -8 \) V, \( V_d = 8 \) V, with the substrate grounded and the source floating. This bias configuration is known to cause gate-induced-drain-leakage (GIDL) current, as well as hole injection into the oxide near the junction transition region. Similarly, we can inject holes near the source junction by interchanging the source and the drain during the GIDL stress. Simultaneous hole injection near both junctions can also be accomplished by setting \( V_d = V_s = 8 \) V during the GIDL stress.

Fig. 7 shows the noise power spectra for a device measured before FN injection (curve 1), after negative-gate FN injection (curve 2), and after subsequent 2-junction GIDL stress (curve 3). Comparing curve 2 with curve 1, apparently the FN injection causes almost three orders of magnitude increase of the noise.
power. Since our charge pumping and subthreshold data (not shown here) indicate that the FN injection has only caused an increase in the interfacial defects of no more than 30 times, we believe that some other factor must be considered. Since we know this particular injection condition causes a higher threshold voltage near the source/drain junctions than in the main channel for this set of devices [14], we suspect that such a dramatic increase of noise could be partly due to the effect of the nonuniform $V_{th}$ distribution along the channel, as described in the THEORY section.

To verify the contribution of channel nonuniformity, we use the 2-junction GIDL-induced hole injection scheme to electrically neutralize some of the trapped electrons in the oxide near the source and the drain junctions so as to bring down the local threshold voltage in these regions. The resulting noise power spectrum (shown as curve 3 in Fig. 7) clearly indicates a significant noise reduction of more than one order of magnitude. Since one would not expect the GIDL stress to cause a significant reduction of the interfacial defects (as also verified by our charge pumping and subthreshold measurements), the observed noise reduction is believed to be due to the removal of the high threshold regions near the junctions.

The following data in Fig. 8 also support the hypothesis of the channel nonuniformity effect. Curves 1 and 2 in Fig. 8 are equivalent to the corresponding curves in Fig. 7. Again, the FN injection should cause a higher threshold voltage near the source/drain junctions, which we believe at least partly responsible for the significant increase in the 1/f noise, according to our theory. Curve 3 is the result after a subsequent drain-side GIDL stress. This GIDL stress causes local hole injection near the drain only, which brings down the threshold voltage in that region. Since there is still a high threshold region near the source, the 1/f noise remains high after this drain-side GIDL stress. In fact, the data (curve 3) indicate a slight increase above curve 2, due probably to the additional damage by the GIDL stress. However, after a subsequent source-side GIDL injection to bring down the threshold voltage near the source injection as well, the 1/f noise becomes dramatically reduced, as indicated by curve 4. These data serve to demonstrate qualitatively the significant impact of channel nonuniformity on the 1/f noise. Note that curve 4 in Fig. 8 is similar in magnitude to curve 3 in Fig. 7, as expected, because in both cases the GIDL stress has removed the high threshold regions near both the source and the drain junctions.

As mentioned previously, our theory is highly simplified, and therefore it is not worthwhile at this point to verify its quantitative validity. However, we believe we have demonstrated qualitatively the key point of this section; i.e., a small region of higher threshold voltage than the rest of the channel could cause a dramatic increase of the drain current noise in a MOSFET.

While in the example described above we used Fowler–Nordheim injection to create the nonuniform channel for the purpose of illustration, one can imagine other causes of channel nonuniformity, such as lateral nonuniformity of doping concentration (especially near the drain and the source junctions), or as a result of channel-hot-carrier damage, which could all give rise to enhanced drain current fluctuations [15]. Both of these cases are expected to be more difficult to control as the dimensions of the MOSFET continue to scale down.

VI. EFFECTS OF FAST INTERFACE STATES

Fig. 9(a) shows a representative time domain trace of the drain current for a small MOSFET measured in weak inversion. A slow RTS of time constants on the order of seconds is clearly observed, and this is the type of RTS's that often appeared in the literature. Note that superimposed on the slow RTS is a high-frequency noisy component, which has generally been ignored. However, if one uses a sufficiently faster sampling rate to resolve the high-frequency noisy component, a fast RTS with time constants on the order of 100 $\mu$s is revealed in this sample, as shown in Fig. 9(b). It should be noted that the amplitude of the fast RTS in Fig. 9(b) is slightly bigger than the amplitude of the slow RTS shown in Fig. 9(a). The reason that the amplitude of the high-frequency "noisy" component in Fig. 9(a) appears to be so small is because of the filtering effect associated with a slow sampling rate.

Such high-frequency RTS's have been attributed to the trapping/detrapping events at the fast interface states [16]. To observe the RTS's arising from fast interface states, the sampling rate must be higher than $1/\tau$, where $\tau$ is the time constant of the interface state. For a typical MOS device, $\tau$ ranges from a few ms (for an interface state near midgap) to a fraction of a $\mu$s (for an interface state near the conduction or the valence band edge) [17]. Therefore, it is much easier to probe the interface states by the RTS measurement when the MOS device is biased in weak inversion (or subthreshold region) than when it is biased in strong inversion. In strong inversion, a sampling frequency of higher than 10 MHz is typically required to observe the RTS's arising from interface states because of their short time constants, which is very difficult experimentally.
We now turn to the effects of fast interface states on the 1/f noise in a MOSFET. To distinguish the contribution of the fast interface states from that of the oxide traps, we performed a set of experiments in which we simultaneously decreased the oxide traps and increased the interface states in a set of MOSFET's, and monitored the changes in the 1/f noise [18], [19]. Because of space limitations, these experiments will not be described here. It suffices to say that strong evidence has been obtained which clearly indicates that the high-frequency noise is due to fast interface states while the low-frequency noise is due to oxide traps [18], [19]. The demarcation frequency depends on the time constant and density of fast interface states: the shorter the time constant and the lower the density, the higher this frequency. In strong inversion, the time constant is so short (less than 1 μs) that the fast interface states usually do not contribute significantly to the 1/f noise in the typical range of frequencies (≤10 kHz) measured. In weak inversion, however, the effect of interface states on the 1/f noise can be quite significant, as we have demonstrated experimentally [18], [19].

In Section V we showed that the current fluctuations are significantly enhanced when there is a nonuniform distribution of the threshold voltages along the channel, and that the region with a higher threshold voltage will be the dominant contributor to the noise. Since for a given n-channel MOSFET the channel region with a higher threshold voltage is also the region that is more weakly inverted, one would expect a greater contribution of interface states to the noise in a device with channel nonuniformity, which is more likely to occur as the channel length further scales down.

VII. SUMMARY

We have shown both theoretically and experimentally that the RTS amplitudes and the 1/f noise in MOSFET's tend to increase as we scale down the device dimensions, and the rate of increase is much faster than the scaling factor. When a nonuniform distribution of threshold voltages exists along the channel, which is more likely to exist in a deep submicron device, the drain current fluctuations are enhanced, with a dominant contribution from the region of a higher threshold voltage. In cases where one small region in the channel has a much higher threshold voltage than the rest, the total noise power density of the device can be increased by a factor of \((L/L_1)^2\), where \(L\) is the channel length of the device and \(L_1\) is the small section of the channel that has the higher threshold voltage. We have also shown that fast interface states can produce RTS's and 1/f noise, although at higher frequencies than those typically produced by oxide traps. Because of the experimental difficulties involved in high-frequency measurements, the contributions from the fast interface states are more easily observable for devices biased in weak inversion. The role of interface states in producing RTS's and 1/f noise would become more important as we move toward technologies of lower power dissipation and/or cryogenic temperature operations.

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REFERENCES


[10] Table II in [5].


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