Electron transport measurements of Schottky barrier inhomogeneities

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We report nonmonotonicities in the low-temperature current versus gate voltage characteristics of PtSi/Si Schottky Barrier metal–oxide–semiconductor field-effect transistors. Direct tunneling through the Schottky barrier is shown to limit the current and be superimposed with resonant peaks and oscillations. These structures are attributed to resonant tunneling through impurities located close to the interface and nonuniformities of the heterojunction. We thus demonstrate barrier height variations in electron transport through a relatively large metal/semiconductor contact area. The inhomogeneities result in different average Schottky barrier heights between devices, and cause height variations as a function of carrier concentration within a metal/semiconductor interface.
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Electron transport in metal–semiconductor contacts is of great technological importance and has been a long-standing topic of research.[1–3] A principle part of this work is devoted to understanding the origin of the bulk Schottky barrier height in order to increase the uniformity of the electrical characteristics from device to device. Traditionally, measurements have used current versus voltage ($I-V$), capacitance–voltage, and photoemission experiments. Recently, ballistic electron emission microscopy (BEEM) techniques demonstrated that nanoscale inhomogeneities give rise to nonideal macroscopic behavior in the $I-V$ characteristics of a diode.[3–7] The scanning tunneling microscope in these experiments, however, allows only very small contact areas to be probed. In this letter, we investigate transport through the Schottky barrier of PtSi/Si contacts by examining the low-temperature current versus gate voltage ($I-V_g$) characteristics in Schottky-barrier metal–oxide–semiconductor field-effect transistors (SBMOSETs). Unlike BEEM experiments, we are able to examine the homogeneity of a relatively large metal/semiconductor contact area.

As shown schematically in Fig. 1, the devices consist of metal silicide contacts instead of $p-n$ junctions. SBMOSFETs have been proposed as an alternative to traditional MOSFETs for sub-100 nm integration because of superior scaling properties and ease of fabrication.[8–11] We recently reported large on/off ratios in bulk silicon devices[12] and a detailed investigation of current transport mechanisms.[13,14] Fabrication was carried out at National Semiconductor in Santa Clara, CA.[10] The relevant devices parameters include: a lightly doped (5×10^{15}) n-type substrate, a 34 Å gate oxide, 135 Å sidewall spacer oxide, and 300 Å of Pt at the source and drain. Measurements were performed using a variable temperature cryostat and HP4145b and Agilent 4156b semiconductor parameter analyzers. The gate and substrate currents were periodically monitored to ensure that leakage currents (<1 pA) were negligible.

The $I-V_g$ equation for direct tunneling at low temperatures can be written as

$$I_{dt}(V_g)=C(V_a)E_{00}(V_g)\exp\left[-\frac{\phi_b}{E_{00}(V_g)}\right], \quad (1)$$

where C is a device specific constant that depends on applied bias V_a, ϕ_0 is the barrier height, and E_{00} is the reduced energy and related to V_g by

$$E_{00}(V_g)=\frac{q\hbar}{2}\sqrt{\frac{N_{\text{eff}}}{\varepsilon_s m^*}}=\frac{q\hbar}{2}\sqrt{\frac{C_{\text{ox}}|V_g-V_t|}{q d_s \varepsilon_s m^*}}, \quad (2)$$

where q is charge, is the Planck constant, m^* is the effective mass, ε_s is the dielectric constant of the semiconductor, N_{eff} is the effective surface concentration in the channel, C_{ox} is the capacitance per unit area of the oxide, $d_s\sim100$ Å is the depth of the inversion layer, and V_t is the threshold voltage. Equation (1) can be derived by the Wentzel–Kramers–

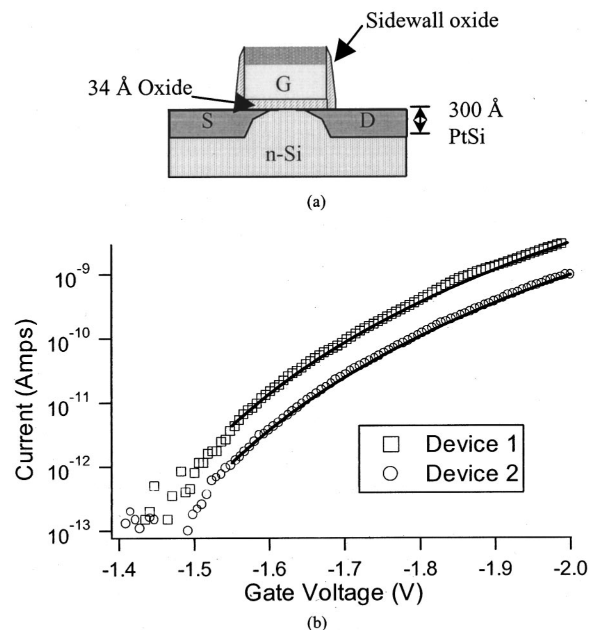

FIG. 1. (a) Schematic of the SBMOSFET. (b) I_d vs V_g characteristics taken at 3.84 K and $V_{\text{ds}}=-5$ mV. The markers indicate the raw data and the solid lines are fits to Eq. (1) with fitting parameters shown in Table I.

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TABLE I. Fitting parameters for characteristics in Figs. 1(b) and 3.

Size (width μm/ length μm)	V_{ds} (V)	ϕ_b (eV)
20/1.67 (Device 1)	−0.005	0.264
20/1.67 (Device 2)	−0.005	0.271
20/1.67 (Device 1)	−0.050	0.260
20/1.67 (Device 2)	−0.050	0.273
20/0.05	−0.050	0.274
2.0/0.05	−0.050	0.269

Brillouin approximation using triangular or parabolic barriers,[14–16] and is valid when $|V_{\mathrm{ds}}| \ll \phi_b$ and $E_{00} \gg kT$. We assume that drain-source bias V_{ds} is dropped equally at both the forward and reverse barriers $(2V_a = V_{\mathrm{ds}})$. The gate bias results in a substantial image force lowering $\Delta\phi$ of the intrinsic barrier ϕ_{bi}, that is taken into account by

$$\Delta\phi = \phi_b - \phi_{bi} = \sqrt{\frac{qE_{\max}}{4\pi\varepsilon_s}} = \left(\frac{2q^3 N_{\mathrm{eff}}\psi_{\mathrm{bs}}}{16\pi^2\varepsilon_s^3}\right)^{1/4}, \tag{3}$$

where ψ_{bs} is the band bending near the metal/semiconductor at the surface.

Figure 1(b) shows the transfer characteristics and fits to Eq. (1) for two devices (width/length$=20\ \mu$m/2 μm) at $V_{\mathrm{ds}} = -5$ mV. We use the exponential fitting parameter to obtain the barrier heights, which are given in Table I. The effective mass is assumed to be $0.56m_0$, the average value obtained from Shubnikov–de Haas oscillations.[17,18] From Table I, we see that device 2, which has a smaller current, has a slightly larger barrier height. We observe an average Schottky barrier height of ~0.269 eV, which is slightly larger than values reported for PtSi/p-type Si (~0.22 eV). This discrepancy may be due to the increase in the silicon band gap at low temperatures. The difference in barrier heights between the two devices can be attributed to nonuniformities in the metal/semiconductor contact. As depicted in Fig. 2, at larger V_{ds} values, device 1 exhibits two types of nonmonotonicities: a resonant peak at larger gate voltages and current oscillations at smaller values.

The resonant tunneling peak can be explained by the presence of a charged impurity situated close to the metal/semiconductor interface, in which resonant tunneling is observed as the gate is energetically swept through the Fermi level. The presence of these "accidental quantum dots" has been explored extensively in previous research,[19–21] but here its proximity to the metal/semiconductor interface effectively changes the average Schottky barrier height. While this peak is barely visible in Fig. 1(b), it resolves into a much larger effect as V_{ds} bias is increased, shown in Fig. 2(a). The exact origin of the impurity is unclear but it is most likely caused by an unintentional acceptor impurity or by a Pt atom that diffused into the depletion width from the silicided contacts. The direct tunneling fit is problematic in the region near the impurity, and temperature cycling resulted in the peak shifting to a higher V_g value. The resonant tunneling peaks have been observed at various positions in gate bias and in five of the ten devices measured.

In Fig. 2(b), current oscillations as a function of V_g are observed for larger V_{ds} values and are attributed to variations in the local potential of the barrier height. At small V_{ds}, bias

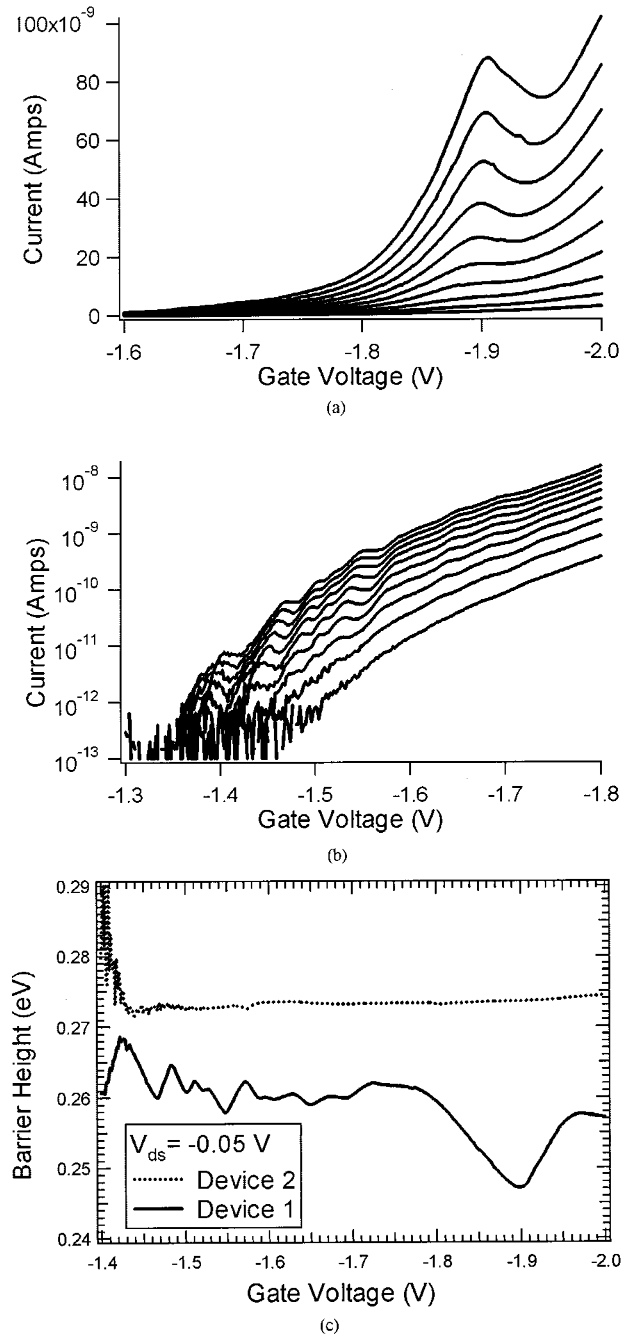

FIG. 2. (a) Characteristics of device 1 taken in V_{ds} steps of −5 mV. The bottom curve is the same as that in Fig. 1(b) and the top curve where $V_{\mathrm{ds}} = -50$ V, shows clear resonant tunneling through a localized state. (b) Log I_{d} vs V_{g} data taken at 3.84 K with V_{ds} values taken in steps of −5 mV. The oscillations for small values of V_g are a result of nonuniformities leading to smaller average Schottky barrier heights than the bulk average. (c) Barrier height vs gate voltage for devices 1 and 2, obtained using the pre-exponential fitting parameter from Eq. (1).

variations are not observable because the net effect as compared to the average barrier height is too weak. As the bias is increased, transport occurs with greater ease and nonmonotonicities appear *before* current flow is dominated by transport through the entire width. Current oscillations were observed in about three of the ten devices measured and always appear at these smaller values of V_g. In Table I, the parameters of the direct tunneling fits at $V_{\mathrm{ds}} = -0.05$ V are compared.

While the values in Table I can be viewed as the average

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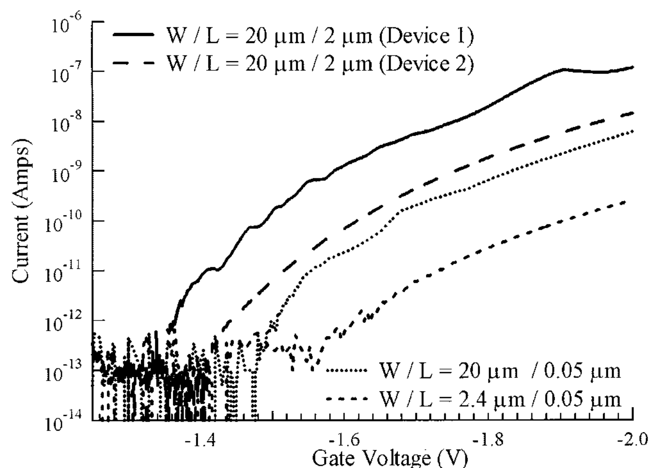

FIG. 3. I vs V_g for different device sizes at $V_{ds}=-50$ mV, fitting parameters are given in Table I.

effective barrier height for a range of carrier concentrations, using the pre-exponential fitting parameter and Eq. (1), we can determine the variation of the barrier height as a function of gate bias. In Fig. 2(c), we thus plot the barrier height as a function of gate voltage for devices 1 and 2. While device 2 exhibits a relatively constant barrier height, device 1 exhibits large variations due to the current oscillations and the resonant tunneling peak. Direct tunneling measurements through SBMOSFETs allows us to obtain both an average effective barrier height and distribution of barrier heights as a function of carrier concentration for metal/semiconductor contacts containing inhomogeneities. This result implies that the same inhomogeneity in metal/semiconductor diodes in which the carrier concentration of the semiconductor is different can result in different barrier heights.

Ten different devices with varying sizes were measured. Most of the long channel devices exhibited either current oscillations or a resonant tunneling peak. Smaller width devices demonstrated less structure than the long channel devices, as depicted in Fig. 3, and thus barrier inhomogeneities become less important in devices with smaller contact areas. Although the inhomogeneities are not observed at room temperature, there is a large effect on the drive currents of the devices. At room temperature, device 1 turns on at an earlier V_g value and has a larger drive current than device 2. Barrier inhomogeneities thus do not effect the physics of room temperature device operation, however, the drive current of SBMOSFETs may be substantially effected because of the resulting modification to the average Schottky barrier height. Nominally doped, ultrasmall width SBMOSFETs should result in more uniform drive currents.

We have shown that low-temperature transport in SBMOSFETs is dominated by direct tunneling and that inhomogeneities lead to variations in the average Schottky barrier height between different devices. This method of investigating transport in Schottky barriers leads to insight in the effect of nonuniformities in metal/semiconductor contacts. In particular, we demonstrate a low-temperature technique by which nonuniformities in a large device area can be probed and show that the carrier concentration can substantially effect the average barrier height. Future research combining gated Schottky barriers and BEEM investigations should lead to a better understanding of the origin of the bulk Schottky barrier height.

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