

Suppression of leakage current in Schottky barrier metal–oxide–semiconductor field-effect transistors

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In this article we investigate the subthreshold behavior of PtSi source/drain Schottky barrier metal–oxide–semiconductor field-effect transistors. We demonstrate very large on/off ratios on bulk silicon devices and show that slight process variations can result in anomalous leakage paths that degrade the subthreshold swing and complicate investigations of device scaling. © 2002 American Institute of Physics. [DOI: 10.1063/1.1425074]

Silicon Schottky barrier metal–oxide–semiconductor field-effect transistors (SBMOSFETs) have been proposed as an alternative to traditional MOSFETs for sub-100 nm integration because of their superior scaling properties and ease of fabrication.^{1–4} While earlier devices have exhibited low drive currents,^{5,6} recent experimental research has shown that the off state leakage current in PtSi/Si SBMOSFETs can be substantial.^{7–11} Other researchers have successfully used SiGe as the source/drain^{3,12} or silicon-on-insulator (SOI),¹³ however this entails either unconventional or more expensive processing. A previous investigation concentrated on PtSi device operation at low temperatures,⁸ and the present work focuses on subthreshold behavior at room temperature. In particular, we present PtSi SBMOSFETs on bulk Si wafers with on/off ratios that are improved by four orders of magnitude. Although these devices are susceptible to anomalous leakage currents that can substantially deteriorate the subthreshold characteristics, we demonstrate that they can be eliminated by slight process variations. This low leakage is also valuable for silicidation of conventional MOSFETs, in which ultrashallow silicided junctions can lead to large leakage currents.¹⁴

The source/drain (S/D) of a SBMOSFET consists only of metal silicide contacts [Fig. 1(a)] which penetrate underneath the gate. The devices were fabricated on *n*-type silicon wafers ($N = 5 \times 10^{15} \text{ cm}^{-3}$) at National Semiconductor (Santa Clara, CA) and were isolated using a simple field oxide growth and etch technique.^{7–9} The gate oxide in this work was 34 Å and the sidewall spacer, formed by rapid thermal oxidation (RTO), had a nominal thickness of either 100 (6 s RTO) or 135 Å (15 s RTO). The small difference in

the RTO time resulted in a large difference in the subthreshold leakage current. After sidewall spacer growth, 300 Å of Pt was sputtered on and PtSi was formed by a 30 min furnace anneal in N₂ at 300 °C. A subsequent selective etch in aqua regia removed any remaining Pt. Except for the difference in RTO processing, the devices were fabricated simultaneously on different 8 in. wafers. Device operation is depicted in Fig. 1(b).

Figure 2 illustrates the transfer characteristics for transistors with width/length = 20 μm/1.7 μm and the different RTO times. The two devices behave quite similarly at room temperature for $|V_g| > |V_t|$, however for smaller gate voltage values the device with the shorter RTO time exhibits substantial leakage current. The low leakage device behaves in the ideal manner depicted in Fig. 1(b). The current is negligible at all electrodes (including the gate) until the barrier at the drain is sufficiently lowered so that transport over the decreased effective hole barrier is possible. In Fig. 3(a) all the currents of the low leakage device are shown and it is clear that the dominant current path is between the source and drain.

In the high leakage device [Fig. 3(b)], the source, drain, and substrate currents are large and constant with the gate voltage until $V_g \sim -0.8 \text{ V}$, when they begin to increase. Large leakage current flows from the drain to the substrate, despite the fact that the substrate is further from the drain than the source, depicted in Fig. 4. The leakage current thus originates *outside* the active device area. More evidence for this result is shown in Fig. 5, where the source current versus gate voltage is plotted for two different device sizes. While there is some deterioration in the subthreshold swing of the low leakage devices, the leakage current in the high leakage devices is nearly identical. The leakage current thus does not depend on the size of the channel length, an observation supported by cross-sectional transmission electron micro-

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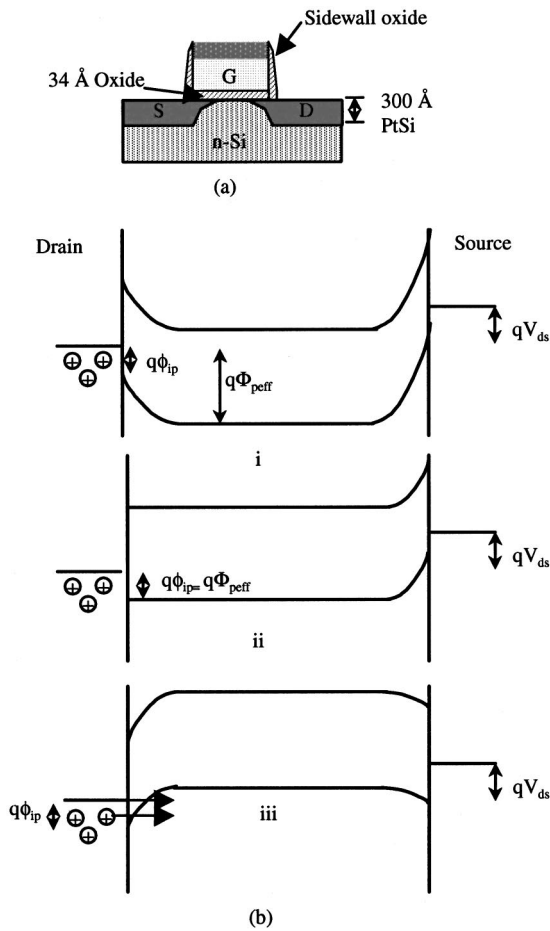


FIG. 1. (a) Schematic of the SBMOSFET (not drawn to scale). (b) Band diagram of device operation using a simple one-dimensional model (i) at $V_g=0$, the effective barrier is $\Phi_{peff} = \phi_{ip} + V_c$ where $\phi_{ip} = 0.22$ eV is the intrinsic p barrier height and V_c is the contact potential. In a low leakage device at sufficiently small V_{ds} carriers cannot surmount the barriers. (ii) With applied V_g the hole barrier is lowered and holes are ejected via thermionic emission into the channel. At $|V_g| \approx 0.93$ V, $\Phi_{peff} \approx \phi_{ip} = 0.22$ eV, as shown in (ii) the hole barrier can be lowered no further. (iii) When $|V_g| > 0.93$ holes can both surmount and tunnel through the source barrier.

graphs XTEM images of the channel in which different RTO times have similar source/drain contact profiles under the gate.⁷ To further investigate the source of this leakage, an ohmic contact was formed to the bottom of the substrate so

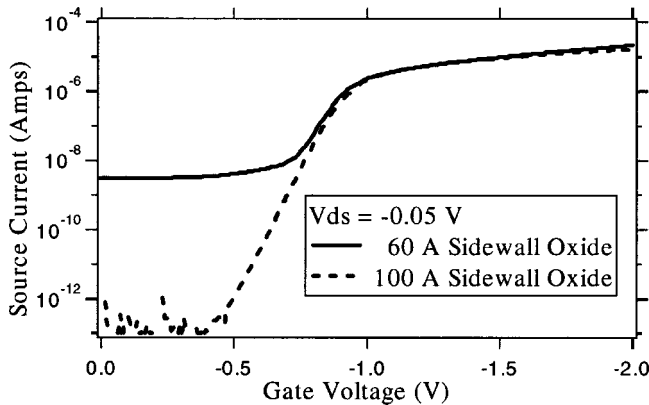


FIG. 2. Room temperature transfer characteristics of the 6s (60 Å oxide) and the 15s (100 Å oxide) RTO devices (width/length=20 μ m/1.7 μ m).

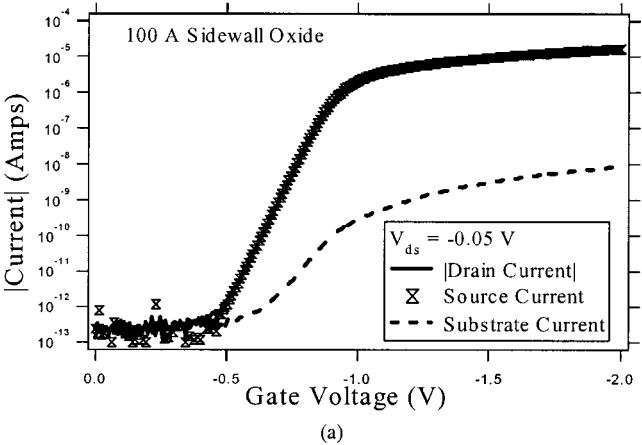
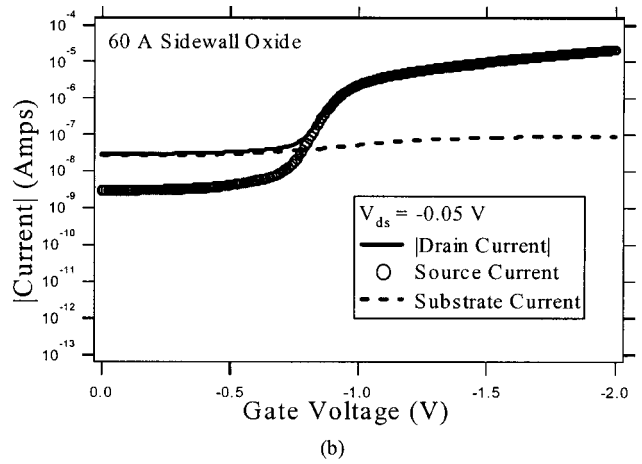


FIG. 3. Room temperature $|I_d|$, I_s , I_{sub} vs V_g for the (a) low leakage and (b) high leakage devices.

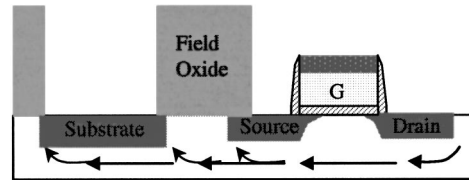


FIG. 4. Schematic of suspected current leakage paths in the thinner sidewall oxide device. The substrate contact consists of a PtSi Schottky barrier surrounded by field oxide, that allows the substrate to remain at the same potential as the source.

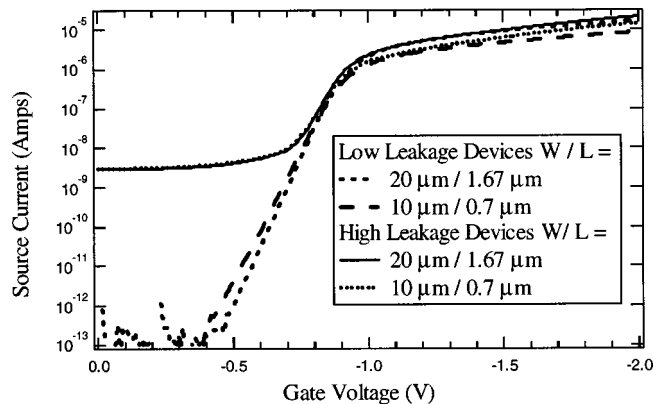


FIG. 5. Subthreshold curves of different size devices at $V_{ds} = -0.05$ V. The low leakage device characteristics scale with the width, but the anomalous leakage plateaus do not. While the low leakage devices reveal some degradation in the subthreshold slope due to a decrease in device size, the effect is masked in the high leakage devices.

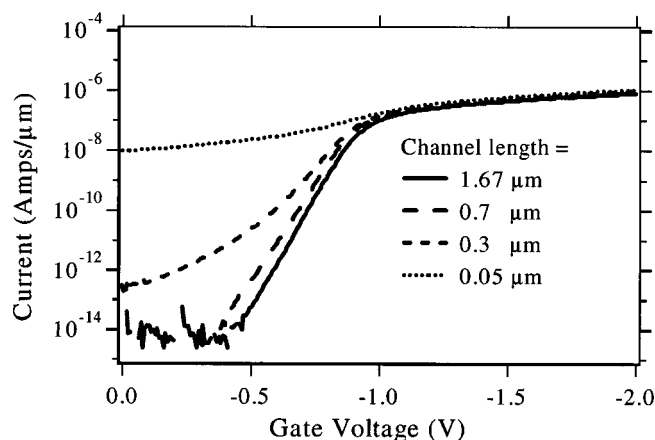


FIG. 6. Transfer characteristics for different size low leakage devices at $V_{ds} = -0.05$ V.

that the forward bias curves and thus the ideality factors could be obtained. While the Schottky contact of the low-leakage device exhibited a near perfect ideality factor of 1.006, the high leakage device exhibited one of 2.24.

Because the leakage current does not depend on the size of the device (Fig. 5) it may be due to an edge effect. While the PtSi contacts at the source and drain are surrounded on one side by rapid thermal oxide and on the other by field oxide, the substrate is completely surrounded by field oxide. The leakage current may thus originate at the sharp edge of the PtSi contact underneath the field oxide (Fig. 4). Previous research on reverse bias Schottky barrier diodes has shown that sharp contact edges result in high electric fields and give rise to large leakage currents.¹⁵ In SBMOSFETs, the profile of the field oxide is very sharp after the etch used to define the source/drain regions. The longer RTO time used to form the sidewall spacers may allow rounding of the field oxide edge. The profile of the PtSi around the field oxide is critically dependent upon the field oxide's edge profile, e.g., a slightly rounder field oxide corner will result in a rounder PtSi corner. The longer RTO time may thus result in a rounder field oxide edge and thus effectively eliminate the leakage current.

From Fig. 5 we see that, if the leakage current is too large, it can mask short channel effects in scaled devices. In previous research it was reported that 50 nm SBMOSFETs that have drive currents similar to or slightly less than conventional *p*-MOSFETs but show large off state leakage currents.⁹ In Fig. 6 we can observe the subthreshold scaling behavior of low leakage devices as the channel length is

scaled from ~ 2 to ~ 50 nm. Here we are clearly able to discern the increase in subsurface punchthrough as the channel length is decreased. The degradation is a result of merging depletion widths in the bulk silicon. In particular, the depletion width due to the PtSi/Si substrate ($N = 5 \times 10^{15} \text{ cm}^{-3}$) interface is $\sim 0.4 \mu\text{m}$ whereas the depletion width at the PtSi/Si surface (at $V_g = 0$ V and $n_s = 1 \times 10^{13} \text{ cm}^{-2}$) is 10 nm.

Record on/off ratios were demonstrated for PtSi SBMOSFETs on bulk silicon. The large off currents typically seen in these devices may be due to sharp edges that arise in the contacts and must be eliminated before considering device scaling. Previous research on very small channel length SBMOSFETs has suggested the use of punchthrough stoppers in order to suppress the short channel effects discussed both here and elsewhere,⁹ however, one must be careful that the method does not exacerbate the high fields found at the sharp edges of the contacts and thus worsen the off-state leakage currents.

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