Superlattices and Microstructures, Vol. 28, No. 5/6, 2000
doi:10.1006/spmi.2000.0954
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Subthreshold and scaling of PtSi Schottky barrier MOSFETs

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(Received 26 July 2000)

We examine the subthreshold behavior of metal oxide semiconductor field effect transistors (MOSFETs) with Schottky barrier (SB) source/drain and large on/off ratios. Thermionic emission dominates the drain current versus gate voltage curves and the sharp turn on is attributed to a decrease in the effective hole barrier with gate bias. We present a simple 1D model and find excellent agreement between the experimentally determined effective barriers and the calculated results. Smaller devices exhibit significantly degraded characteristics, which are attributed to a sub-surface punch-through of the source and drain depletion widths at zero gate bias. Implications for SBMOSFETs are discussed.

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Key words: Schottky barrier source drain MOSFET, thermionic emission, subthreshold behavior, MOSFET scaling.

1. Introduction

Schottky barrier MOSFETs (SBMOSFETs) have been proposed as an alternative to traditional MOSFETs for sub-100 nm integration because of excellent scaling properties and ease of fabrication [1–4]. While earlier devices exhibited low drive currents [6, 7], recent experimental research has focused on either device fabrication or operation at low temperatures [8–10]. Other researchers have successfully used SiGe as the source/drain [11], or concentrated on silicon-on-insulator (SOI) devices [12, 13]. Previously, characterization of transistors on bulk silicon has been hampered by large leakage currents and correspondingly poor on/off ratios. It has been speculated that the leakage currents are due to sharp edges at the source/drain contacts that result in regions of high electric field and thus leaky Schottky barriers [14]. We report pSBMOSFETs with large on/off ratios that enable us to examine the subthreshold behavior. The scaling of devices ranging in channel length from 1.7 μm down to 30 nm is also discussed.

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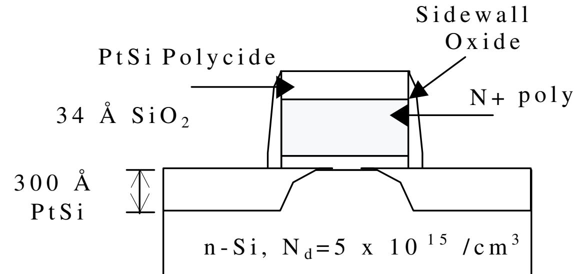

Fig. 1. Schematic of a SBMOSFET (not drawn to scale).

Where the source/drain (S/D) of a traditional MOSFET consists of doped regions, the S/D of an SBMOSFET consists of metal silicide contacts (see Fig. 1). Fabrication was carried out on lightly doped (5×10^{15}) n-type wafers using a conventional self-aligned process and a 34 Å gate oxide. The sidewall spacer was formed by a rapid thermal oxidation (RTO) and a nominal thickness of 135 Å was obtained. We deposited 300 Å of Pt at the S/D and a subsequent anneal allowed the formation of PtSi [5, 9]. The devices were fabricated at National Semiconductor in Santa Clara, CA, using an 8-in. fabrication process and measurements were performed on about 20 devices of the same size and processing conditions to ensure reproducible results.

2. Long channel devices

The device operation is based on modifying the barriers as a function of gate bias, as depicted in Fig. 2. Unlike conventional MOSFETs where the subthreshold current is dominated by the diffusion of carriers in the channel [15], in SBMOSFETs, it is dominated by thermionic emission. In the off state the large effective p barrier ϕ_{peff} blocks the transport of carriers into the channel, Fig. 2A. ϕ_{peff} consists of two parts: the intrinsic p barrier ϕ_{ip} and the contact potential ϕ_{c} ($\phi_{\mathrm{peff}} = \phi_{\mathrm{ip}} + \phi_{\mathrm{c}}$). As $|V_{\mathrm{g}}|$ increases, ϕ_{c} is reduced and carriers have enough thermal energy to surmount the barrier. Threshold, V_{t} (Fig. 2B), occurs when $\phi_{\mathrm{c}} = 0$ and subsequent increases in current with gate bias are due to an increase in the tunneling through the barrier (Fig. 2C). The transfer characteristics for a long channel device are shown in Fig. 3. The subthreshold current can be modeled using a 2D thermionic emission equation, derived using the traditional method [15] but with a 2D density of states and an effective barrier ϕ_{peff}. The result is:

$$I = wA^{**}T^{3/2} \exp(-q\phi_{\mathrm{peff}}/kT)\{\exp(qV_{\mathrm{ds}}/kT) - 1\} \tag{1}$$

where w is the physical channel width, A^{**} is the 2D effective Richardson constant, k is the Boltzmann constant, T is temperature, and V_{ds} is the drain source bias. Note that ϕ_{peff} depends on V_{g} and that the equation is only strictly valid when tunneling and channel resistance do not dominate the transport, e.g. when $V_{\mathrm{g}} < V_{\mathrm{t}}$.

One can determine the experimental effective barrier height by variable temperature measurements. Using a Janis cryostat and a HP4145 semiconductor parameter analyzer, a series of subthreshold characteristics were taken in 5° intervals from 297 to 180 K. From an Arrhenius plot, heights were obtained for each point in the I_{d}–V_{g} curve and thus an experimental barrier as a function of gate voltage was determined. The result is shown as the dashed curve in Fig. 4. For $|V_{\mathrm{g}}| < 0.8$ V, the barrier height appears to increase with decreasing gate bias. This can be attributed to the resolution of the current and fit as the temperature is decreased. At $|V_{\mathrm{g}}| = 0.95$ V, threshold is reached and the intrinsic barrier is found to be ~0.22 eV. For $|V_{\mathrm{g}}| > 0.95$ V, the experimental barrier continues to decrease, but with a different slope than previously. Modeling in this regime is much more complicated because the transport through the barrier is due to both thermionic emission

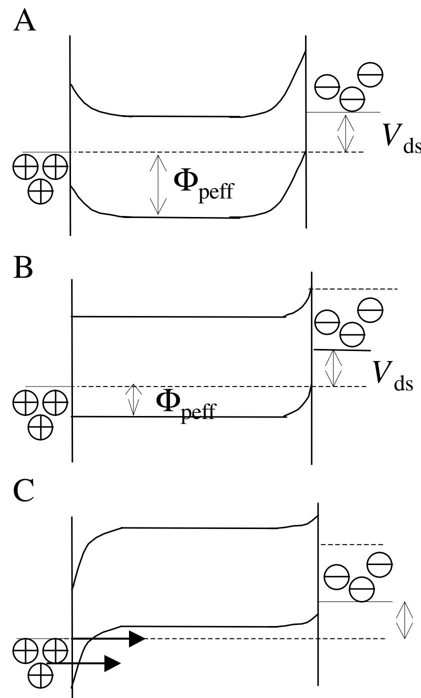

Fig. 2. Band diagram of device operation using a simple 1D model. A, At $V_g = 0$, the effective barrier is $\phi_{peff} = \phi_{pi} + \phi_c$ where $\phi_{pi} = 0.22$ eV is the intrinsic p barrier height and ϕ_c is the contact potential. In a low leakage device at sufficiently small V_{ds}, carriers cannot surmount the barriers. B, With applied V_g the hole barrier is lowered and holes are ejected via thermionic emission into the channel. At $|V_g| \approx 0.93$ V, $\phi_{peff} \approx \phi_{pi} = 0.22$ eV, as shown in the figure, the hole barrier can be lowered no further. C, When $|V_g| > 0.93$, holes can both surmount and tunnel through the source barrier.

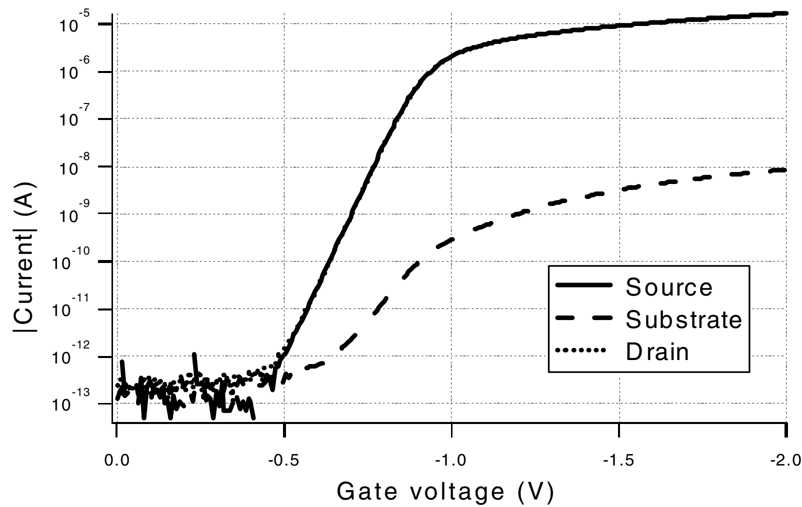

Fig. 3. Transfer characteristics of the long channel SBMOSFET (width = 20 μm, length = 1.67 μm) at room temperature and $V_{ds} = -0.05$ V. Note that the source and drain currents are equal and opposite and that the substrate current is much smaller in magnitude.

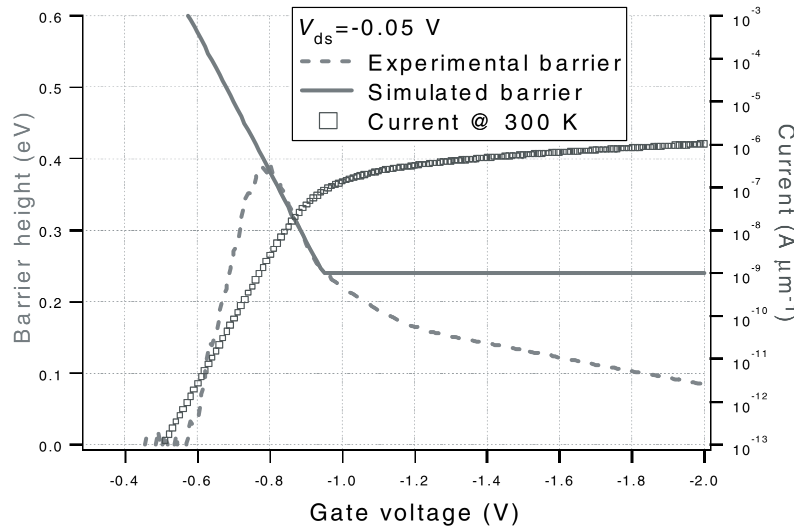

Fig. 4. Barrier heights (left y-axis) determined experimentally and by simulation. $|I_d|$ at 298 K (right y-axis) is also shown. Note that the simulated barrier height matches the experimental barrier height quite nicely in the range expected ($0.8 < |V_g| < 0.95$). This graph can be used to obtain the leakage current at a given effective barrier height and thus is useful in SBMOSFET design.

and thermal assisted tunneling and because the channel resistance becomes more important. Despite these caveats, the barrier height for $|V_g| > |V_t|$ does in fact fit well to the thermionic emission equation, indicating that even beyond threshold it is an important component of the current.

We now propose a simple 1D model to obtain a theoretical effective barrier in the subthreshold regime. A classical MOS depletion approximation [15] was used to determine the surface concentration n_s and thus the contact potential and effective barrier height were obtained. Note that this method assumes that: (a) most of the V_{ds} bias is dropped at the barrier and thus the MOS capacitor equations can be used to obtain n_s; (b) the majority of current flow will be at the surface where the carrier concentration is the greatest and therefore the 2D effects due to transport underneath the surface of the MOS capacitor are negligible; (c) the surface is non-degenerate; and (d) quantum mechanical effects can be neglected. The results of the theoretical barrier heights are shown in Fig. 4 as the solid line. In this simple model we have used only the thermionic emission equation and thus once V_t is reached, the simulated versus experimental heights differ.

Within the resolution of the measurement ($|V_g| > 0.8$ V) and the accuracy of the simulated barrier height ($|V_g| < 0.95$ V), the agreement between the two barrier heights is quite good. For $|V_g| < 0.8$ V, the simulated barrier provides an estimate of the barrier height and when plotted with the corresponding leakage current, we obtain the leakage current corresponding to a given barrier height. For instance, an initial effective barrier height of 0.6 eV corresponds to ~pA μm^{-1} of current and thus is sufficient to restrict leakage current into the channel. For an SBMOSFET that does not exhibit the short channel effects discussed in the next section, this curve is valuable for V_t and subthreshold design because it allows one to determine the leakage current for a given ϕ_{peff}. This correspondence between effective barrier height and leakage current is also valuable for silicidation of conventional MOSFETs, where ultrashallow silicided junctions can lead to large leakage currents [16].

3. Scaling and short channel effects

We now turn to the device characteristics of scaled SBMOSFETs. Figures 5 and 6 depict the subthreshold behavior and short channel effects for different device sizes. The 0.7 μm channel length device exhibits only

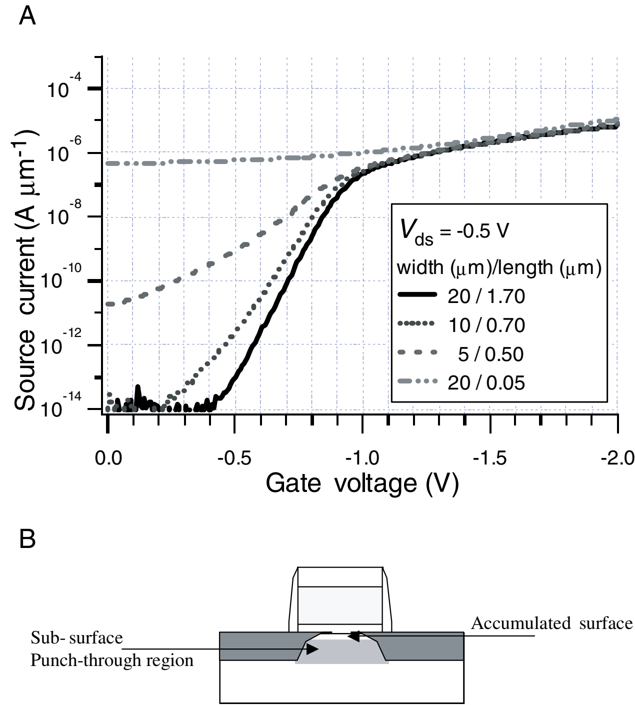

Fig. 5. A, Transfer characteristics for different size devices. B, Schematic depicting where the sub-surface punch-through originates.

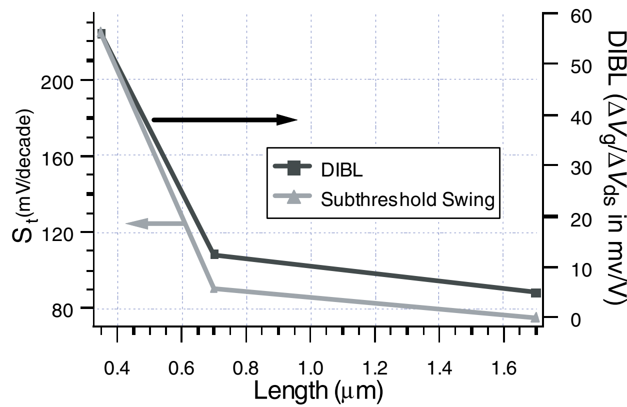

Fig. 6. DIBL and subthreshold swing versus gate length.

small degradations in drain induced barrier lowering (DIBL), and subthreshold swing. In the 0.3 μm channel length device, there is significant degradation in the subthreshold swing and DIBL. Finally, the smallest device is completely punched through at $V_g = 0$, evidenced by normalized leakage current at $V_g = 0$ being equal to the current of the larger channel devices at $V_g = V_t$. These short channel effects at first seem to contradict simulations that predict SBMOSFETs can be scaled down to very small dimensions [1–4].

The scaling behavior can be explained, however, by a sub-surface punch-through. The depletion width due to the PtSi/Si substrate ($N = 5 \times 10^{15}$) interface is $\sim$0.4 μm. In comparison, the depletion widths of the PtSi/Si at the semiconductor surface (at $V_g = 0$ and $n_s = 1 \times 10^{19}$) is 10 nm. Degraded device characteristics thus occur when the two depletion widths at the PtSi/Si substrate interfaces begin to overlap and result in a reduced contact potential ϕ_c. DIBL is caused by the reduced sub-surface barrier height. Similarly, the degraded subthreshold swing results from the presence of different current paths: transport in the channel and transport sub-surface. In the smallest device, $\phi_c = 0$ at $V_g = 0$ and thus the device characteristics in the off state are severely degraded.

In order to obtain the excellent scaling behavior that simulations have predicted [1–4], the sub-surface punch-through should be eliminated. One possible method is engineering the source drain such that the PtSi contacts are highly tapered: close together near the channel in order to define a small channel length and further apart in the sub-surface region to prevent punch-through. Another option is the use of punch-through stoppers, which would decrease the depletion widths underneath the gate by increasing the doping concentration. SOI is also an attractive alternative because a thin-enough silicon layer would eliminate the sub-surface region altogether. Recent experimental research on SOI wafers obtained excellent subthreshold characteristics in channel lengths of 35 nm [12] and 20 nm [13]. We believe that the subthreshold behavior of scaled devices in which the sub-surface punch-through is eliminated would be very similar to the low leakage long channel devices we demonstrated in the first section of this paper and in Ref. [13].

4. Conclusions

We have investigated the subthreshold behavior of long channel SBMOSFETs and shown how to determine a correspondence between the effective barrier height and the subthreshold leakage current, a variable that is important for device design. Similarly, we have seen that sub-surface leakage in the device can put severe limitations on the scaling of SBMOSFETs. These results indicate that tapered source/drain contacts, ultra-thin SOI or punch-through stoppers would be greatly advantageous in designing very small SBMOSFETs.

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