

# Making Silicon Nitride Film a Viable Gate Dielectric

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(Invited Paper)

**Abstract**— To extend the scaling limit of thermal SiO<sub>2</sub> in the ultrathin regime when the direct tunneling current becomes significant, members of this author's research team at Yale University, in collaboration with the Jet Process Corporation, embarked on a program to explore the potential of silicon nitride as an alternative gate dielectric. In this paper, high-quality silicon nitride (or oxynitride) films made by a novel jet vapor deposition (JVD) technique are described. The JVD process utilizes a high-speed jet of light carrier gas to transport the depositing species onto the substrate to form the desired films. The film composition has been determined to consist primarily of Si and N, with some amounts of O and H. Metal-nitride-Si (MNS) capacitors based on the JVD nitride films deposited directly on Si exhibit relatively low densities of interface traps, fixed charge, and bulk traps. The interface traps at the nitride/Si interface exhibit different properties from those at the SiO<sub>2</sub>/Si interface in several aspects. In contrast to the conventional CVD silicon nitride, the high-field  $I-V$  characteristics of the JVD silicon nitride fit the Fowler-Nordheim (F-N) tunneling theory over four to five orders of magnitude in current, but do not fit at all the Frenkel-Poole (F-P) transport theory. This is consistent with the much lower concentration of electronic traps in the JVD silicon nitride. Results from the carrier separation experiment indicate that electron current dominates the gate current with very little hole contribution. Both theoretical calculation and experimental data indicate that the gate leakage current in JVD silicon nitride is significantly lower than that in silicon dioxide of the same equivalent oxide thickness. The breakdown characteristics of the JVD nitride are also respectable. Compared to their MOSFET counterparts, MNS transistors exhibit reduced low-field transconductance but enhanced high-field transconductance, perhaps due to the presence of border traps. As expected, the JVD silicon nitride films exhibit very strong resistance to boron penetration and oxidation at high temperatures. These properties, coupled with its room-temperature deposition process, make JVD silicon nitride an attractive candidate to succeed thermal SiO<sub>2</sub> as an advanced gate dielectric in future generations of ULSI devices.

**Index Terms**— Dielectric films, MOS capacitors, MOSFET's, thin films, vapor deposition, ultra-large-scale integration

## I. INTRODUCTION

**T**HERMALLY grown SiO<sub>2</sub>, the currently prevailing gate dielectric for Si-based MOS devices, possesses remarkable electronic properties that are unmatched by other materials. However, it will someday outlive its usefulness as the device dimensions, including the gate oxide thickness, continue to shrink in each successive generation of new

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integrated circuit technology, and an alternative gate dielectric must be found in the foreseeable future if the scaling trend is to be sustained.

In the course of searching for such an alternative gate dielectric, researchers at Yale University, in collaboration with researchers at the Jet Process Corporation (JPC), developed a process for synthesizing silicon nitride films based on a novel Jet Vapor Deposition (JVD) technique [1]–[12], and found that the electronic properties of the JVD nitride, deposited directly on Si at room temperature, approached those of thermal SiO<sub>2</sub> in several key aspects, but with a lower gate leakage current density for the same equivalent oxide thickness (EOT) in the ultrathin ( $\leq 5$  nm) regime. The higher dielectric constant of the JVD nitride (nearly twice that of the thermal SiO<sub>2</sub>) allows a thicker gate dielectric to be used to achieve the same device performance. Other properties of the JVD nitride, such as its high resistance to impurity diffusion and oxidation, also make it attractive as a gate dielectric.

The JVD process relies on supersonic jets of a light carrier gas such as helium to transport depositing vapor from the source to the substrate, and has been used to synthesize a wide variety of thin films of metals, semiconductors, and insulators [1]–[8]. Because of the separation of the constituent depositing species, and their short transit times, there is very little chance for gas-phase nucleation. We believe the high impact energies of the depositing species also contribute to the improved film quality.

This paper reviews the progress on the JVD silicon nitride research, and summarizes the properties of the JVD nitride films as we know them. Since silicon nitride has been studied for decades [13]–[22], and numerous attempts to develop the CVD silicon nitride into a viable gate dielectric directly on Si have all failed due to poor nitride/Si interface properties as well as high densities of bulk traps, it is curious as to what makes the JVD nitride so different. While the answer to that question is still being sought, it is probably safe to say that the deposition technique itself must play an important role.

## II. THE JVD PROCESS: A BRIEF DESCRIPTION

The JVD strategy of using jets in low vacuum, fast flows for film deposition was originated by Schmitt and Halpern [1]–[3] of the Jet Process Corporation (JPC), with whom we have an ongoing collaboration. As shown in Fig. 1, the jet that carries the depositing species is formed in a nozzle contained within a flow system pumped by a high-speed mechanical pump (see Fig. 1). It has been shown that, when the pressure in the nozzle over that in the chamber exceeds a critical ratio (typically  $\geq 2$ ), the gas exiting the nozzle will be supersonic [1], [23]. As a

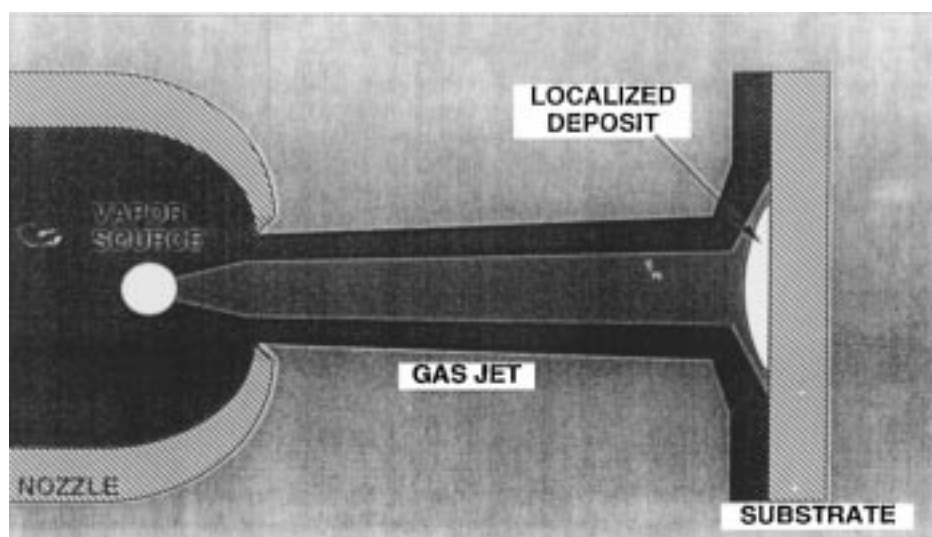


Fig. 1. Schematic representation of a jet vapor source.

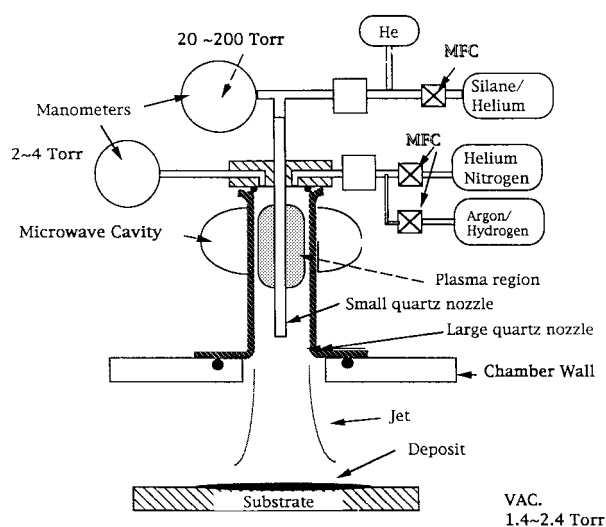


Fig. 2. Schematic representation of the dual-nozzle jet vapor source for silicon nitride deposition (U.S. Patent 5336672).

reference, a supersonic jet expansion of helium at 25 °C has a velocity of approximately 1 km/s. A source of vapor containing the desired depositing species is placed within the throat of the nozzle. The jet of carrier gas entrains the vapor generated in the nozzle throat and convects it rapidly down stream to the surface of the substrate where it deposits to form a thin film. Since the depositing species possess the same supersonic speed as that of the helium carrier gas, the kinetic energies of these species (which are proportional to their masses) could be up in the order of 1 eV.

For the deposition of silicon nitride, we use a coaxial dual-nozzle jet vapor source, as schematically shown in Fig. 2. Highly diluted silane from the inner nozzle and  $N_2 + He$  from the outer nozzle flow into a discharge region sustained by a microwave cavity. The gaseous plasma is sustained only in the outer nozzle, as the pressure in the small inner nozzle is maintained sufficiently high to suppress plasma formation and premature silane dissociation within it. Energetic nitrogen

species (including atomic nitrogen) generated in the plasma and silane molecules are both carried by the sonic He jet toward the substrate where they form silicon nitride. The jet convection of vapor overcomes diffusion limitations on mass transport, and the deposition is highly directed, localized, and efficient. Because of the high kinetic energy of the impinging depositing species, intentional substrate heating is not necessary. Film uniformity across a large area can be achieved by scanning the substrate relative to the jet source(s). In our present research setup (see Fig. 3), we combine both rotational and translational motions of the substrate to achieve a thickness uniformity within  $\pm 5\%$  across a 6-in wafer, and a better uniformity should definitely be readily achievable with a production machine. The deposition rate and film composition are controlled by the  $SiH_4/He$  and the  $SiH_4/N_2$  ratios as well as their flow rates, which critically affect the film properties.

### III. SAMPLE FABRICATION AND CHARACTERIZATION

In the early phase of this research, we investigated a wide range of deposition rates produced by various combinations of deposition parameters, and found that films with best electrical properties were produced at a low rate of 1–3 Å/min in our single-jet research machine. Therefore, unless otherwise specified, all of the JVD silicon nitride samples to be reported in this paper were made at such a low rate. Also, all of the JVD silicon nitride films were deposited at room temperature.

Ellipsometric measurements were made more or less routinely after deposition, especially during the initial phase of our process development effort, to get an idea of the relative thickness and the index of refraction. The etch rate in BOE (buffered oxide etchant) was also frequently taken and correlated with the index of refraction data. FTIR measurements were performed on relatively thick ( $\geq 50$  nm) samples deposited on double-side polished Si wafers to increase the signal/noise ratio. Optical absorption measurements were made on samples deposited on quartz substrate with a spectrophotometer covering the wavelength range of 190–900 nm. Film stress measurements were made with a laser beam reflection

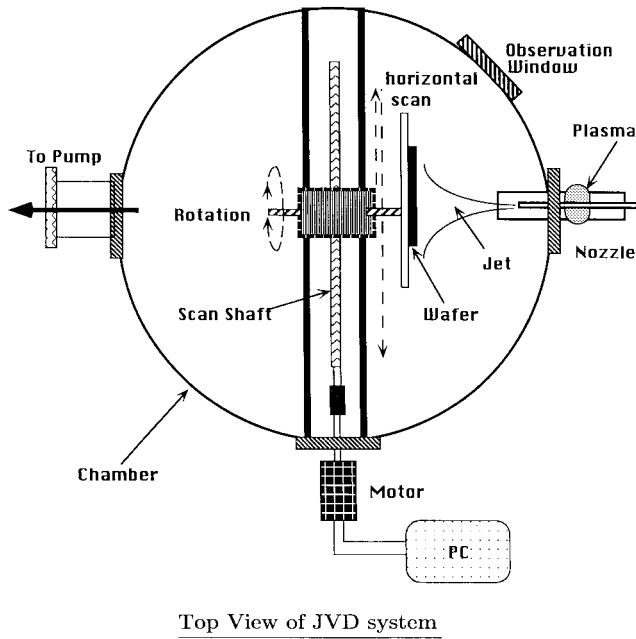


Fig. 3. Top view of the JVD silicon nitride deposition chamber used in this study.

technique. We also sent samples out for high-resolution TEM, Auger profiling, and AFM measurements.

For electrical measurements, metal-nitride-Si (MNS) capacitors were formed by the following procedure. After the nitride deposition, the wafers were annealed in dry  $N_2$  at  $800^\circ C$  for 30 min. Then  $\sim 3000 \text{ \AA}$  of aluminum was thermally evaporated on the front side, followed by photolithography to define the gate electrodes. The fabrication concluded with back-side metallization and annealing either in forming gas ( $5\% H_2 + 95\% N_2$ ) or in water vapor at  $400^\circ C$  for 30 min. The water vapor annealing (WVA) treatment has been shown to improve the properties and reliability of nitride/Si interface [8], while it does not have any noticeable effect on thermal oxide.

Aluminum-gate n-channel and p-channel MNS field-effect transistors were made by adding field oxidation, source-drain diffusion, and contact etching steps to the MNS capacitor process described above. Aluminum-gate MOSFET's with thermal oxide as the gate dielectric were also made at the same time for comparison.

In addition, a full CMOS run has been completed as a joint project with a major semiconductor company based on its  $0.35\text{-}\mu m$  technology coupled with Yale's JVD silicon nitride gate dielectric, and the results have been published [24].

Standard  $C-V$ ,  $G-V$ , and  $I-V$  measurements were used to investigate the electrical properties of the MNS capacitors, and constant-current stress experiments were conducted to evaluate their trapping properties, their resistance to hot-carrier damage, and their charge-to-breakdown characteristics.

#### IV. RESULTS AND DISCUSSIONS

Since ultimately the electrical properties are most relevant for the intended applications, they will be presented first.

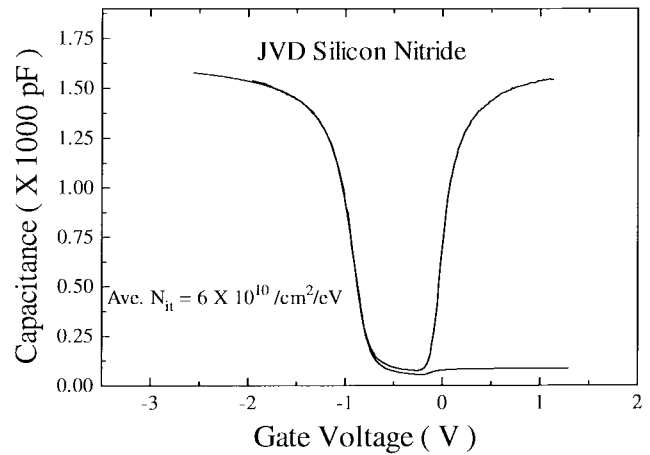


Fig. 4. High-frequency and quasi-static  $C-V$  curves for an MNS capacitor with a JVD silicon nitride of  $EOT = 4.2 \text{ nm}$ .

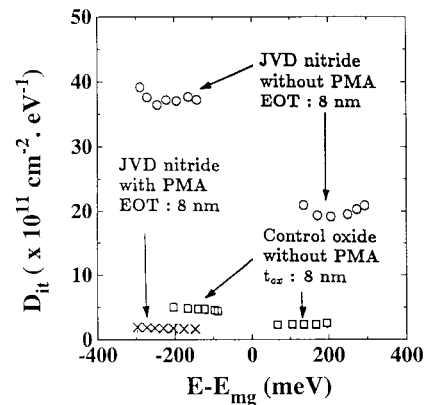


Fig. 5. Interface-trap densities of MNS capacitors before PMA (circles) and after PMA (crosses). The data for MOS capacitors before PMA (squares) are also included for comparison. Data above midgap were obtained on n-type samples, while below midgap were obtained on p-type samples.

Fig. 4 shows a pair of high-frequency and quasi-static  $C-V$  curves for an MNS capacitor with a JVD nitride film of  $4.5 \text{ nm}$  of equivalent  $SiO_2$  thickness (EOT). There is no discernible hysteresis in the high-frequency  $C-V$  curve when swept back and forth along the voltage axis. These results are comparable to quality MOS capacitors, and certainly much better than any other MNS capacitors made of conventional CVD silicon nitride reported in the literature. Such high-quality interface afforded us the opportunity to study in much more detail than before the properties of interface traps in a MNS system [9]. Some of these properties are reported below.

Fig. 5 shows the interface-trap density distribution  $D_{it}$  as obtained by the ac conductance technique [25], for a MNS capacitor before and after post-metal anneal (PMA). One can see that the  $D_{it}$  level is reasonably low for this sample after PMA, and we are now routinely getting  $D_{it}$  down to the mid  $10^{10}/\text{cm}^2\text{-eV}$  range. The data for a MOS control sample are also included for comparison.

Fig. 6 shows the time constants of the interface traps for eight silicon nitride capacitors that underwent different processing conditions. For example, samples #1-6 each received a somewhat different nitride deposition condition and none had received PMA, while samples #7 and #8 both had

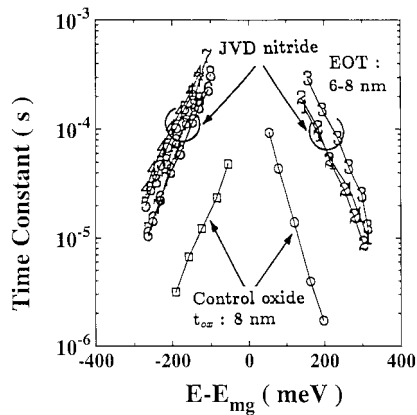


Fig. 6. Time constants associated with interface traps. Curves 1-3: 3 n-type MNS capacitors processed differently without PMA; Curves 4-6: 3 p-type MNS capacitors processed differently without PMA; Curves 7 and 8: 2 p-type MNS capacitors after PMA. Two lower curves: data for MOS capacitors.

received PMA. The corresponding data for the thermal oxide samples are also shown for comparison. Two salient features can be noted in this figure: 1) the time constants of nitride samples tend to group together, despite the different processing histories and 2) the time constants of the nitride samples are one to two orders of magnitude longer than the thermal oxide samples. More details of the interface traps can be found in our earlier publication [9].

Fig. 7(a) shows a family of drain current curves of an N-channel MNS transistor with EOT of 3.8 nm while Fig. 7(b) shows the corresponding transconductance characteristics. This device received WVA treatment as the PMA step. The data for a control MOSFET are also included for comparison. Note that both sets of data have been normalized with respect to the gate EOT in order to have a fair comparison. One can see that the low-field transconductance is lower for the nitride sample, but its high-field transconductance is higher than that of the oxide sample. This behavior is qualitatively similar to devices made of oxynitride gate materials [26], and may be attributed to carrier trapping by the slow interface traps (or border traps [27]) near the nitride/Si interface, as described below [26].

In the low field region, the trapping of carriers by the border traps causes a reduction of the transconductance in the steady state because of the reduction of a significant fraction of the total number of carriers. At high fields, the channel carrier concentration is very high and nearly unaffected by losing a few carriers to the border traps. On the other hand, the lateral distribution of electron trapping could be in such a way as to cause a smoothing of the electronic roughness of the interface as felt by the conducting carriers, resulting in a higher carrier mobility in the high field region. This could happen if trapping takes place preferentially in regions where there were high Coulomb attractive fields before the trapping causes partial neutralization of such fields. This hypothesis is being verified.

The data for the P-channel devices are shown in Fig. 8(a) and (b), where the transconductance for the MNS device is also lower than that for the MOS device at low fields, but higher at high fields.

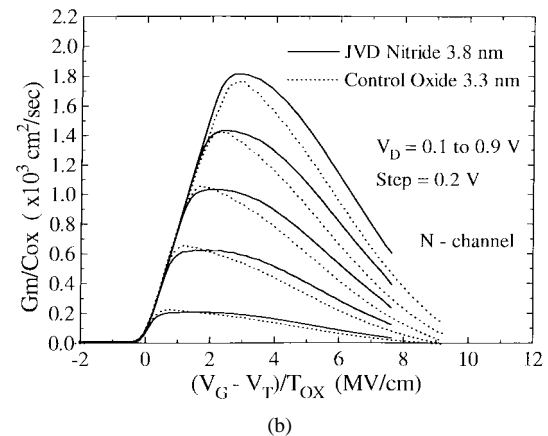
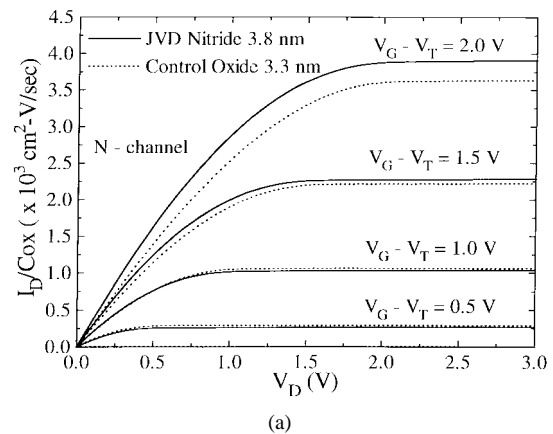


Fig. 7. Transistor characteristics of an n-channel MNS transistor with EOT of 3.8 nm, in comparison to the data for a MOSFET sample: (a) drain current characteristics and (b) transconductance characteristics. All data are normalized with respect to the EOT of the gate dielectric.

Since CVD silicon nitride films typically contain very high densities of bulk traps, we were pleasantly surprised by our results on the JVD silicon nitride films. Fig. 9 shows the result from a constant-current stress experiment. Based on the saturation voltage shift (of order of 30 mV), we estimate a trap density in the  $10^{11}/\text{cm}^2$  range, which is comparable to the values for quality thermal  $\text{SiO}_2$ , but much lower than CVD silicon nitrides.

Fig. 10(a) shows a histogram of the breakdown fields for a set of MNS capacitors with EOT of 4.2 nm, while Fig. 10(b) shows the corresponding time-to-breakdown data under a very high field of 13.5 MV/cm. These data are comparable to high-quality thermal  $\text{SiO}_2$ .

The  $I-V$  characteristics of the MNS capacitors fit Fowler-Nordheim (F-N) plot very well, as exemplified by the data in Fig. 11, where  $J$  is the current density and  $E$  is the equivalent oxide field. Using an effective mass of 0.5 times the free electron mass, we calculated a barrier height of 2.1 eV from the slope of the straight line. Other MNS capacitors show similar barrier height values from their  $I-V$  characteristics.

Since in the conventional CVD silicon nitride the dominant current component is due to the Frenkel-Poole (F-P) conduction mechanism, it is very interesting that the JVD nitride shows primarily F-N tunneling mechanism. We believe the

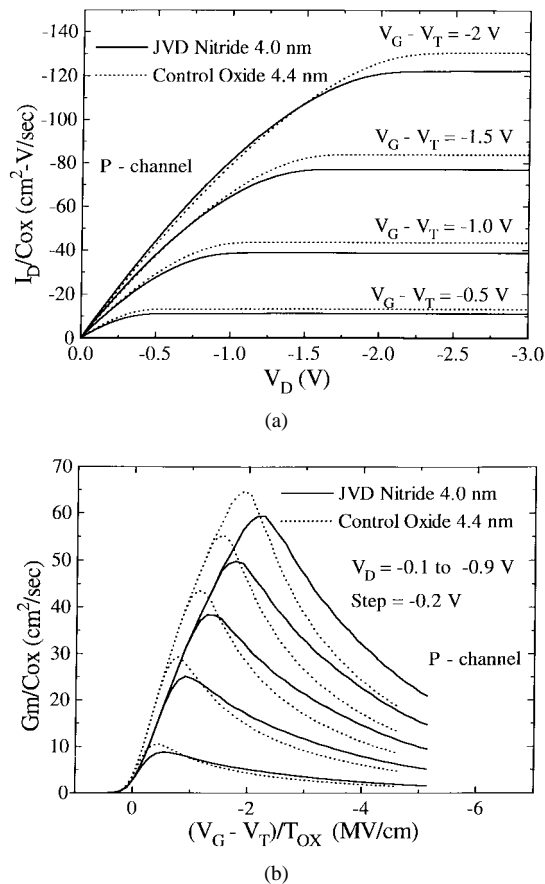


Fig. 8. Transistor characteristics of a p-channel MNS transistor with EOT of 4.0 nm, in comparison to the data for a MOSFET sample: (a) drain current characteristics and (b) transconductance characteristics. All data are normalized with respect to the EOT of the gate dielectric.

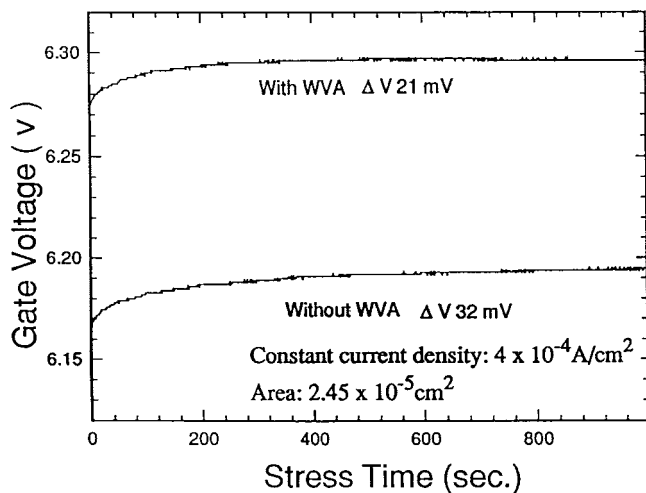


Fig. 9. Gate voltage as a function of time during constant current stress experiment for a MNS capacitor with a JVD silicon nitride. The upper curve is for a sample that had received water-vapor anneal (WVA) while the bottom one is for a sample that had not received WVA.

lack of traps in the JVD nitride is probably responsible for this, because the F-P conduction requires a high density of traps.

The fact that the dominant conduction mechanism in the JVD nitride is tunneling is also confirmed by its relatively

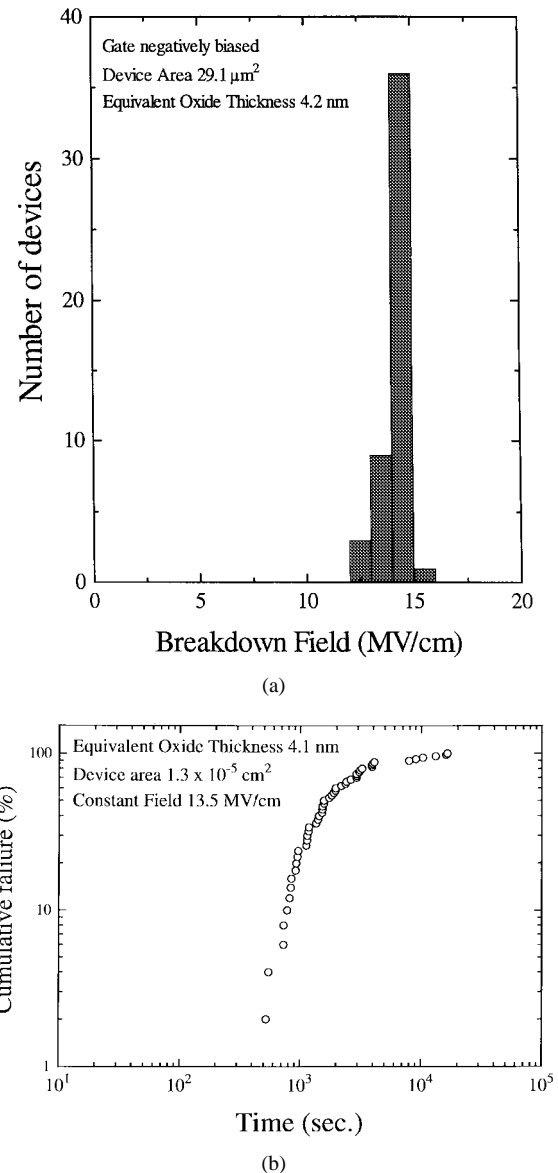


Fig. 10. Breakdown characteristics of MNS capacitors with JVD nitride of 4.2 nm: (a) breakdown field distribution and (b) time-to-breakdown distribution under a constant field of 13.5 MV/cm.

weak temperature dependence, as shown in Fig. 12. As a comparison, the CVD nitride shows a much stronger temperature dependence.

To find out whether both electrons and holes contribute significantly to the conduction mechanism in JVD nitride, we did an experiment based on the well known carrier-separation technique [14] by the use of a n-channel field-effect transistor. When the gate is biased positively with respect to the inverted channel as well as source/drain, the measured gate current should consist of electron current supplied by the source/drain, plus hole current going to the substrate. Our experimental results, shown in Fig. 13, indicate that the substrate current is less than 5% of the total throughout the voltage range studied, suggesting that the dominant gate current is electron current with little hole contribution.

Next I will compare the JVD nitride against the thermal oxide in the ultrathin regime. Our theoretical calculations

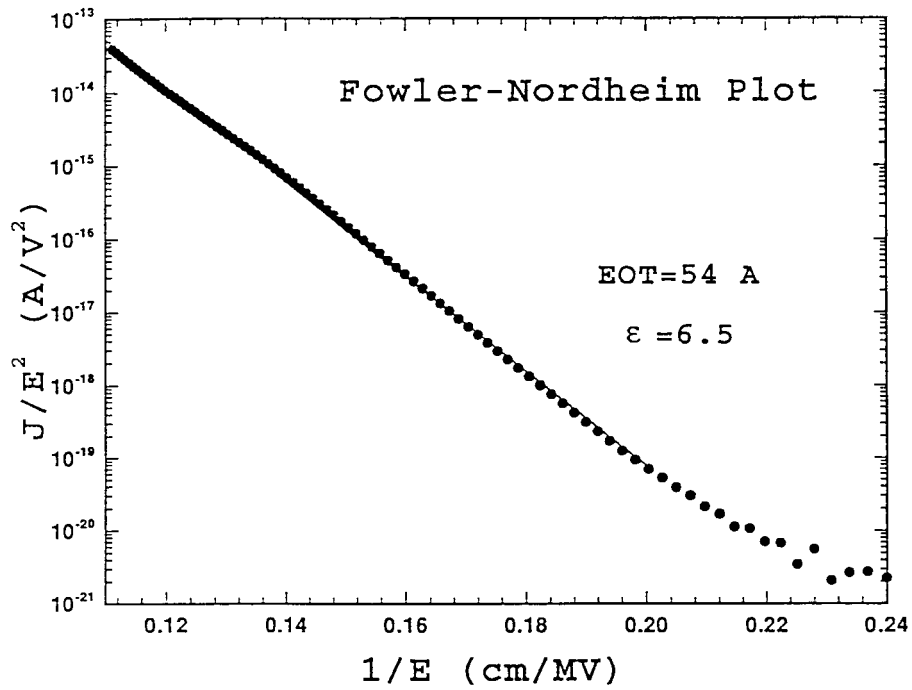


Fig. 11. Fowler-Nordheim plot for a MNS capacitor with a JVD silicon nitride.

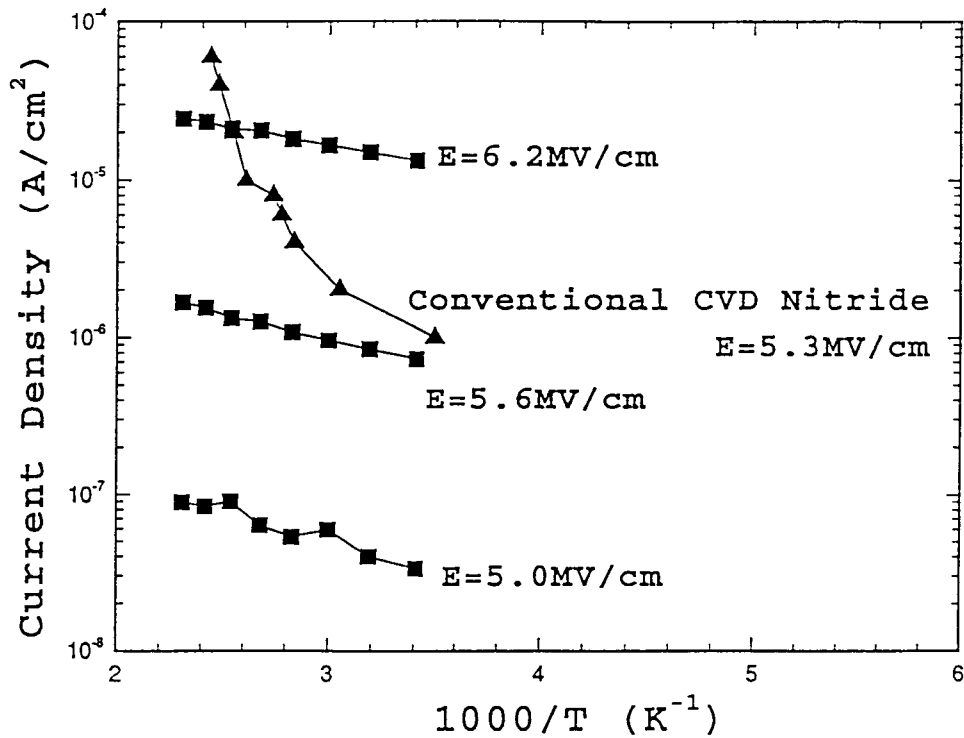


Fig. 12. Temperature dependence of the current through JVD silicon nitride is a lot weaker than that through CVD silicon nitride.

indicate that, if tunneling is the dominant current transport mechanism rather than F-P process, then the gate leakage current should be substantially lower for the nitride when compared with the thermal SiO<sub>2</sub> of the same equivalent thickness [7]. Fig. 14 shows an example where the dielectric constant of the nitride is assumed to be 6.5, which is a reasonable assumption based on our experimental results. Note that the kink in each curve corresponds to the

transition from direct tunneling to F-N tunneling as the dominant transport mechanism. One can see that, for a given equivalent oxide thickness, the leakage current is substantially lower in the nitride, especially in the direct tunneling regime, where the difference is several orders of magnitude. By assuming a higher dielectric constant for the nitride, the calculation showed even lower nitride current [7].

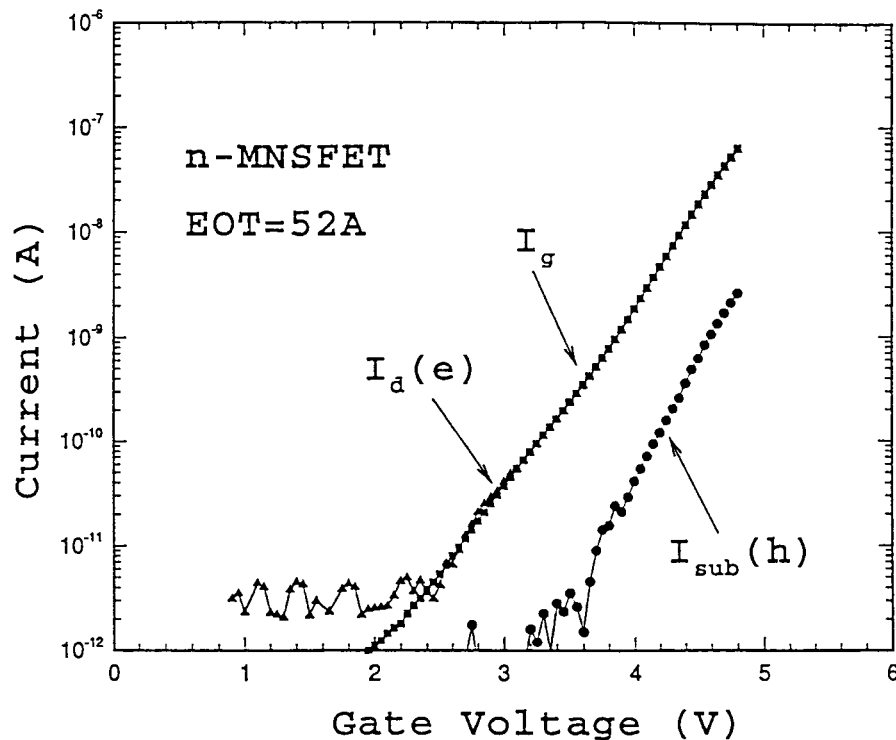


Fig. 13. Gate current consists of electron current (measured as drain current) and hole current (measured as substrate current). The data indicate predominantly electron current.

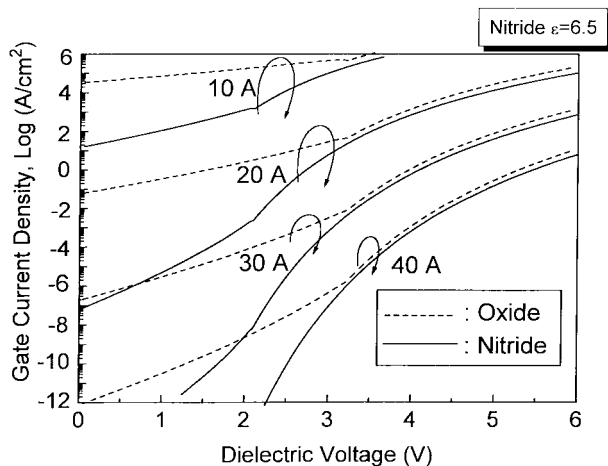


Fig. 14. Calculated tunneling currents for silicon nitride and thermal  $\text{SiO}_2$  of three EOT's.

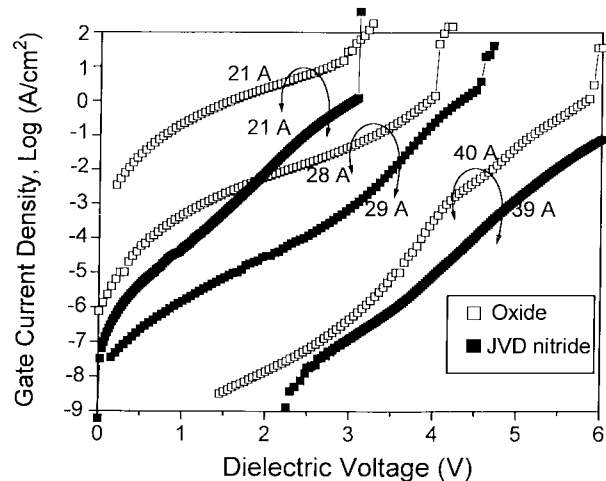


Fig. 15. Experimentally measured gate leakage currents for three JVD nitride films as compared to the data for three thermal  $\text{SiO}_2$  films of similar thicknesses.

Fig. 15 shows the leakage currents measured in three JVD nitride films of 2.1, 2.9, and 3.9 nm of EOT, respectively. For comparison, the data for thermal  $\text{SiO}_2$  of comparable thicknesses are also included. The data clearly indicate a lower leakage current through the nitride for a given oxide equivalent field, in qualitative agreement with the theoretical prediction. In the low-field regime, the leakage currents in the nitride films are not as low as what the tunneling calculations have predicted. We suspect that the F-P conduction mechanism has not been entirely eliminated in these nitride films.

The reason that the tunneling current is much lower in silicon nitride for a given EOT, despite its lower barrier height than  $\text{SiO}_2$ , is because of its larger physical thickness (nearly

twice as thick as  $\text{SiO}_2$ ) which more than offsets the effect of the barrier height difference.

One possible near-term application of the JVD silicon nitride which utilizes its low-leakage current feature is to replace the ONO dielectric for the storage capacitors in DRAM's without the need for the top and bottom oxides. To investigate this possibility, we made MNS capacitors on  $n^+$  poly-Si (300 nm thick, deposited by LPCVD on  $n^-$ -Si substrate). Except for the substrate, these MNS capacitors were processed exactly the same way as those on single-crystal Si substrates.

Fig. 16 compares the current-density versus electrical-field (J-E) curves between the JVD nitride films and conventional

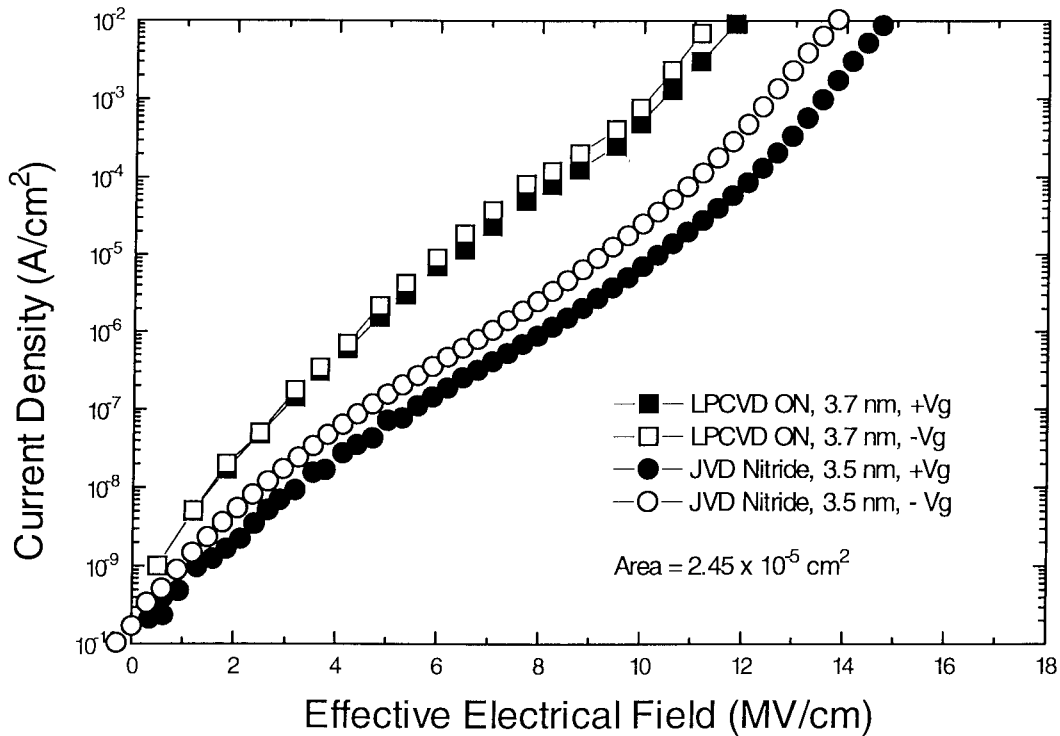


Fig. 16. A comparison of gate leakage current between JVD nitride and CVD ONO [28], both on poly-Si electrode.

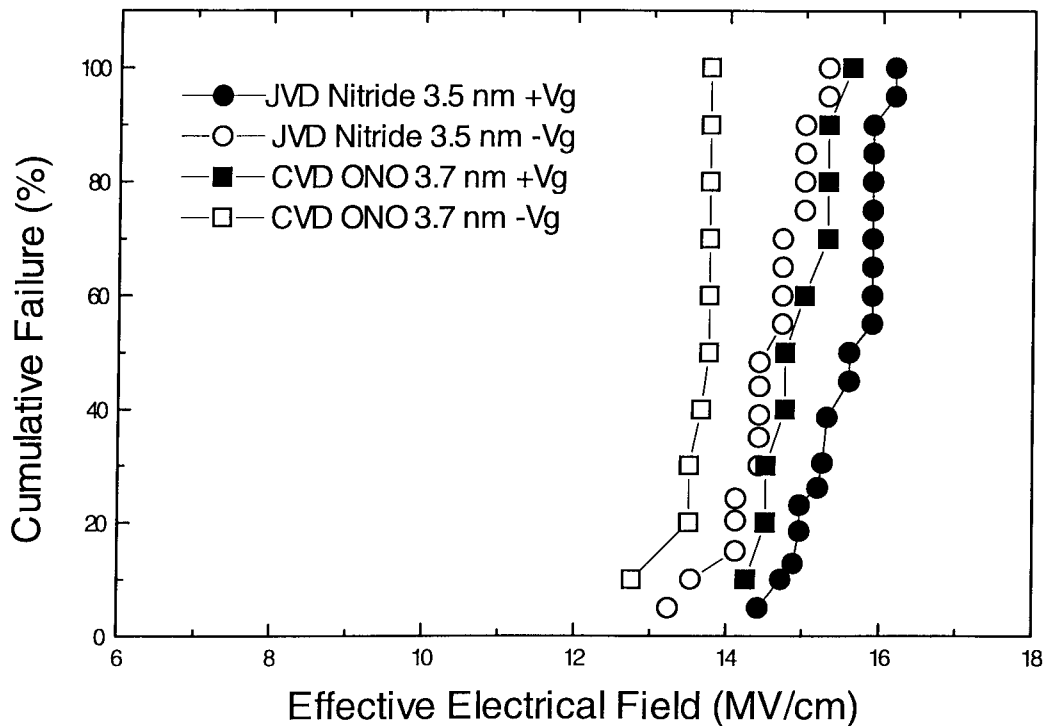


Fig. 17. A comparison of breakdown field distribution between JVD nitride and CVD ONO [28], both on poly-Si electrode.

LPCVD ONO films [28]. A significantly lower leakage current is observed for the JVD nitride film even without the intentional top and bottom oxides. This is consistent with our results obtained on single-crystalline Si substrates. At a voltage of 2 V, the corresponding effective electric field is 2.85 MV/cm

for EOT of 3.5 nm. For the JVD nitride, the current density at 2.85 MV/cm and  $-2.85$  MV/cm are  $5.1 \times 10^{-9}$   $\text{\AA}/\text{cm}^2$  and  $2.0 \times 10^{-8}$   $\text{\AA}/\text{cm}^2$ , respectively, safely fulfilling the requirement of less than  $2.0 \times 10^{-7}$   $\text{\AA}/\text{cm}^2$  of leakage current density at the operating electric field for 256 Mb DRAM.

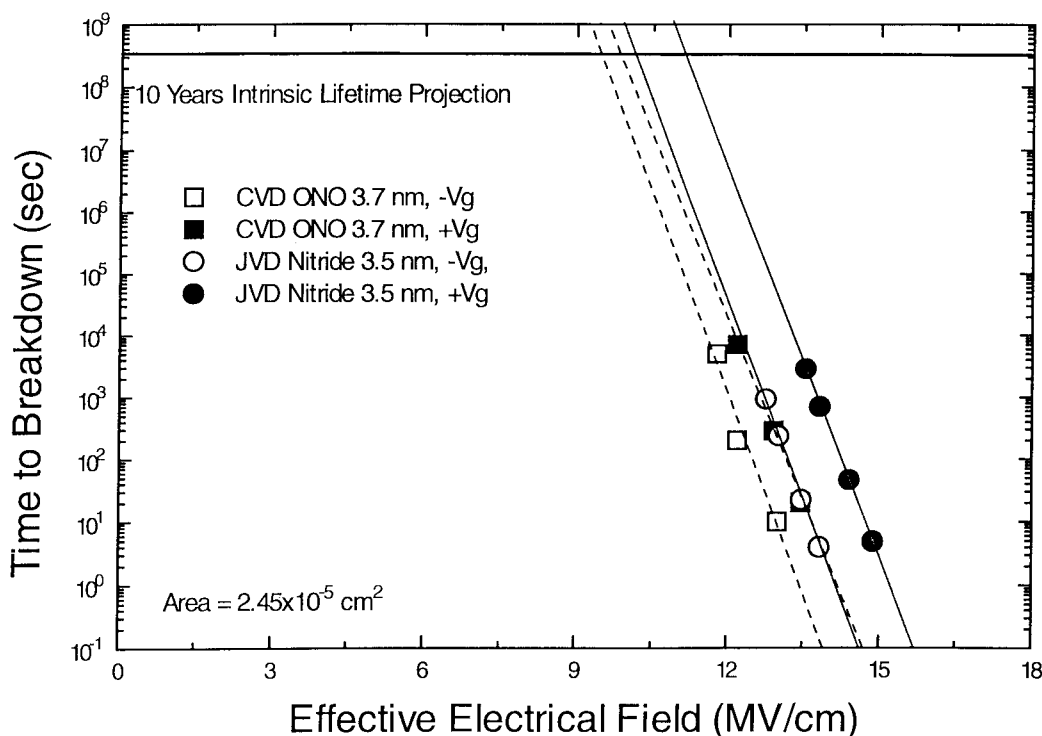


Fig. 18. A comparison of intrinsic lifetime projection between JVD nitride and CVD ONO [28], both on poly-Si electrode.

These results, to our knowledge, are significantly better than any other previously published NO or ONO films deposited on polysilicon substrates [28], [29].

The cumulative failure rates under ramp voltage test for JVD nitride capacitors and conventional LPCVD ONO capacitors [28] are compared in Fig. 17. For both polarities, the JVD nitride films show a higher breakdown field with a tight distribution.

The ten-year intrinsic lifetime projection for the JVD nitride is shown in Fig. 18, where a comparison is made with the conventional LPCVD ONO stack films [28]. It can be seen that more than 9 MV/cm of either polarity can be applied to the JVD nitride film without causing failure in ten years, and that the time-to-breakdown is at least one order of magnitude longer for the JVD nitride when compared with the conventional ONO films at a given electric field.

We have measured the film stress of the JVD nitride on Si by use of the laser-beam reflection method to determine the wafer curvature. Our results indicate that, for a 50-nm film, the as-deposited stress is  $\sim 3.2 \times 10^9$  dyne/cm<sup>2</sup> (tensile), which is similar to thermal oxide stress in magnitude but different in sign. After 800 °C annealing in N<sub>2</sub> for 30 min, which is our typical post-deposition annealing process, the film stress is reduced by an order of magnitude ( $\sim 10^8$  dyne/cm<sup>2</sup>), and becomes difficult to measure with our technique.

High-resolution TEM as well as AFM data show that the JVD nitride/Si interface is very smooth (comparable to the starting Si wafer surface). Such data also allow us to determine the physical thickness, which when combined with our  $C-V$  data, enable us to determine the relative dielectric constant of the JVD nitride as being in the range of 6.5–7.2.

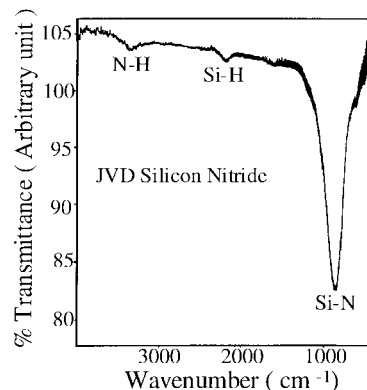


Fig. 19. FTIR spectrum of a JVD silicon nitride film.

Fig. 19 shows the FTIR spectrum of a JVD silicon nitride film which exhibits the expected SiN bonds. The hydrogen concentration, as manifested by the NH and SiH signals, is relatively low as compared to the CVD nitride, which may be partly responsible for the low trapping properties and low leakage current of the JVD nitride, as it has been reported that the trap density increases with hydrogen concentration in CVD silicon nitrides [15]–[18]. One interesting fact worth reporting here is that, unlike the PECVD nitride, the FTIR spectrum of the JVD nitride looks pretty much the same with or without the 800 °C post-deposition anneal, suggesting that the Si–H and N–H bonds in the JVD nitride are very stable, and may not act as trapping centers.

Fig. 20 shows the Auger depth profiles of a JVD silicon nitride film deposited on Si. One can see that, in addition to the Si and N signals, which are expected, there is a fair

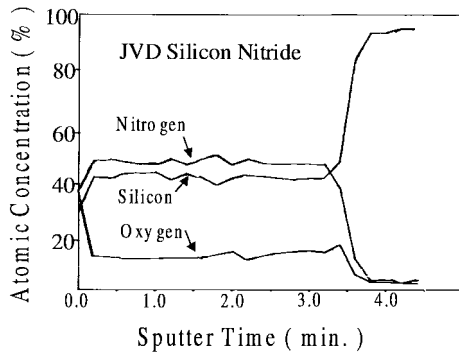


Fig. 20. Auger depth profile of a JVD silicon nitride film deposited on Si.

amount of oxygen uniformly distributed throughout the depth of the film. We suspect that this oxygen comes either from the poor vacuum environment of our deposition chamber, which is evacuated by a rough pump, or from the quartz nozzle. The effects of this oxygen on the film properties remain to be systematically studied.

We have also studied the resistance of the JVD silicon nitride film to boron penetration. Our data indicated that, for JVD nitride films of  $\sim 4$  nm in EOT, no detectable boron penetration took place at a temperature as high as  $1000^\circ\text{C}$  for as long as 30 min, while a 4.3-nm thermal  $\text{SiO}_2$  control sample showed more than two orders of magnitude increase in the surface doping concentration. As an example, Fig. 21(a) shows that the boron drive-in step performed at  $1000^\circ\text{C}$  for one hour has caused the  $CV$  curves of the MOS capacitor to become “shallower” and the minimum capacitance to increase. A subsequent calculation indicated that the effective doping concentration increased from  $5 \times 10^{15}$  to  $1.2 \times 10^{18} \text{ cm}^{-3}$  due to boron penetration. In contrast, the MNS sample with 4.0 nm of JVD nitride exhibits no detectable change after the same boron drive-in step, as shown in Fig. 21(b).

## V. SUMMARY

Although silicon nitride has been widely used in integrated circuits for several decades, numerous attempts to make it a gate dielectric to replace thermal  $\text{SiO}_2$  have not met with success, despite its obvious advantages of higher dielectric constant and strong resistance to impurity diffusion. This situation may be changing due to the advent of the JVD silicon nitride. MNS capacitors, made of the JVD silicon nitride deposited on Si substrates, exhibit a number of properties that are attractive for ULSI applications, including low densities of interface as well as bulk traps, low leakage current, high breakdown strength, high resistance to hot-carrier damage, high resistance to boron penetration, and high resistance to oxidation. Compared to their MOSFET counterparts, MNS-FET's made of JVD silicon nitride exhibit reduced low-field transconductance and enhanced high-field transconductance.

The current transport properties in JVD silicon nitride differ significantly from those in CVD silicon nitride in at least two aspects: 1) electron conduction dominates in JVD nitride, with very little hole contribution and 2) F-N tunneling, instead of F-P conduction, dominates the current transport in JVD nitride. Based on the above, we used electron tunneling theory

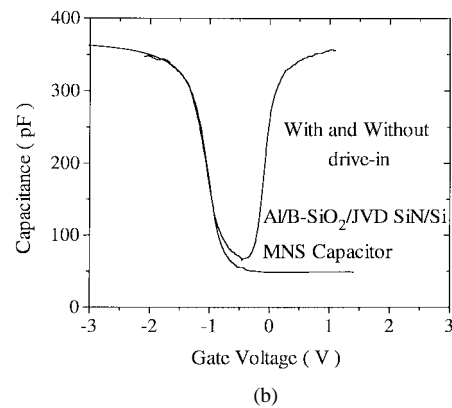
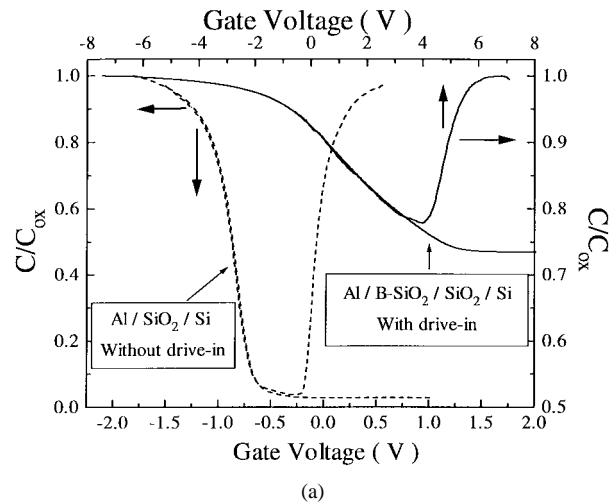


Fig. 21.  $CV$  curves before and after high-temperature boron drive-in step for (a) MOS capacitor with  $\text{SiO}_2$  gate dielectric and (b) MNS capacitor with JVD nitride gate dielectric.

to calculate the  $I-V$  characteristics of the JVD nitride over a thickness range in the ultrathin regime, and found the leakage currents to be significantly lower than in thermal  $\text{SiO}_2$  of the same EOT's. Experimental data verifying this trend have been obtained.

FTIR spectra of the JVD silicon nitride show predominantly S-N bonds, with small amounts of Si-H and N-H bonds. The hydrogen concentrations estimated from the FTIR spectra are lower than those in typical CVD nitrides, which may be partly responsible for JVD nitride's improved electrical properties. Auger depth profiling data indicate the presence of a few percent of oxygen throughout the depth of the JVD nitride film, although no oxygen was intentionally added. High resolution TEM images show very smooth nitride/Si interface, and laser-beam wafer curvature measurements show relatively low stress of the JVD nitride film deposited on Si. Ultrathin JVD silicon nitride films exhibit very strong resistance to boron penetration and oxidation at high temperatures. Many of the aforementioned properties, coupled with the room-temperature deposition process, are attractive for a variety of applications, and more work is underway to understand better what makes the JVD silicon nitride so different from the CVD silicon nitride.

From this author's perspective, the JVD silicon nitride process can be easily integrated with the existing CMOS

process flow, and there does not seem to exist any significant obstacle for its implementation. The only undesirable feature that is apparent with the research machine at this time, the low throughput, is not fundamental to the JVD nitride process, and more than an order of magnitude improvement in the throughput should be readily achievable in a production machine.

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#### REFERENCES

- [1] B. L. Halpern, "Fast flow deposition of metal atoms on liquid surfaces," *J. Colloid Interface Sci.*, vol. 86, pp. 337-341, 1982.
- [2] J. J. Schmitt and B. L. Halpern, "Method and apparatus for the deposition of solid films of material from a jet stream entraining the gaseous phase of said material," U.S. Patent 4 788 082, 1988.
- [3] ———, "Method for microwave plasma assisted supersonic gas jet deposition of thin films," U.S. Patent 5 356 672, 1994.
- [4] C. L. Hwang, B. A. Chen, T. P. Ma, J. W. Goltz, Y. Di, B. L. Halpern, and J. J. Schmitt, "Ferroelectric Pb(Zr,Ti)O<sub>3</sub> thin films prepared by gas jet deposition," *J. Integr. Ferroelectr.*, vol. 2, pp. 221-224, 1992.
- [5] D. Wang, T. P. Ma, J. Goltz, B. Halpern, and J. Schmitt, "High quality MNS capacitors prepared by jet vapor deposition at room temperature," *IEEE Electron Device Lett.*, vol. 13, pp. 482-484, Sept. 1992.
- [6] X. W. Wang, T. P. Ma, G. J. Cui, T. Tamagawa, J. W. Goltz, S. Kareci, B. L. Halpern, and J. J. Schmitt, "Highly reliable silicon nitride films made by jet vapor deposition," *Jpn. J. Appl. Phys.* vol. 34, pt. 1., no. 2B, pp. 955-958, 1995.
- [7] X. W. Wang, Y. Shi, T. P. Ma, G. J. Cui, T. Tamagawa, J. Goltz, B. Halpern, and J. Schmitt, "Extending gate dielectric scaling limit by use of nitride or oxynitride," in *1995 Symp. VLSI Technol. Dig. Tech. Papers*, pp. 109-110.
- [8] X. Wang, M. Khare, and T. P. Ma, "Effects of water vapor anneal on MIS devices made of nitrated gate dielectrics," in *1996 Symp. VLSI Technol. Dig. Tech. Papers*, pp. 226-227.
- [9] A. Mallik, X. W. Wang, T. P. Ma, G. J. Cui, T. Tamagawa, J. Goltz, B. Halpern, and J. Schmitt, "Interface traps in jet vapor deposited silicon nitride-silicon capacitors," *J. Appl. Phys.*, vol. 79, no. 11, pp. 8507-8511, 1996.
- [10] Y. Shi, X. W. Wang, T. P. Ma, G. J. Cui, T. Tamagawa, B. L. Halpern, and J. J. Schmitt, "Ultrathin nitride/oxide stack dielectric produced by *in situ* jet vapor deposition," in *Proc. 1997 Int. Symp. VLSI-TSA*, pp. 172-176.
- [11] M. Khare, X. Guo, X. W. Wang, T. P. Ma, G. J. Cui, T. Tamagawa, B. L. Halpern, and J. J. Schmitt, "Ultrathin silicon nitride gate dielectric for deep-sub-micron CMOS devices," in *1997 Symp. VLSI Technol. Dig. Tech. Papers*, pp. 51-52.
- [12] X. Guo, X. W. Wang, T. P. Ma, G. J. Cui, T. Tamagawa, B. L. Halpern, and J. J. Schmitt, "The use of jet-vapor deposited silicon nitride for scaled DRAM applications," in *Proc. 1997 Int. Symp. VLSI-TSA*, pp. 193-197.
- [13] B. E. Deal, E. L. MacKenna, and P. L. Castro, "Characteristics of fast surface states associated with SiO<sub>2</sub>-Si and Si<sub>3</sub>N<sub>4</sub>-SiO<sub>2</sub>-Si structures," *J. Electrochem. Soc.*, vol. 116, pp. 997-1005, 1969.
- [14] A. S. Ginovker, V. A. Gristzenko, and S. P. Sinitza, "Two-band conduction of amorphous silicon nitride," *Phys. Stat. Sol.(a)*, vol. 26, pp. 489-495, 1974.
- [15] V. J. Kapoor, R. S. Bailey, and H. J. Stein, "Hydrogen-related memory traps in thin silicon nitride films," *J. Vac. Sci. Technol.*, vol. A1, no., pp. 600-603, 1983.
- [16] S. Fujita, T. Ohishi, T. Toyoshima, and A. Sasaki, "Electrical properties of silicon nitride films plasma-deposited from SiF<sub>4</sub>, N<sub>2</sub>, and H<sub>2</sub> source gases," *J. Appl. Phys.*, vol. 57, no. 2, pp. 426-431, 1985.
- [17] M. Maeda and H. Nakamura, "Hydrogen bonding configurations in silicon nitride films prepared by plasma-enhanced deposition," *J. Appl. Phys.*, vol. 58, no. 1, pp. 484-489, 1985.
- [18] K. Alloert, A. Van Calster, H. Loos, and A. Lequesne, "A comparison between silicon nitride films made by PCVD of N<sub>2</sub>-SiH<sub>4</sub>/Ar and N<sub>2</sub>-SiH<sub>4</sub>/He," *J. Electrochem. Soc.*, vol. 132, pp. 1763-1766, 1985.
- [19] W. R. Knolle and J. W. Osenbach, "The structure of plasma-deposited silicon nitride films determined by infrared spectroscopy," *J. Appl. Phys.*, vol. 58, no. 3, pp. 1248-1254, 1985.
- [20] D. V. Tsu, G. Lucovsky, and M. J. Mantini, "Local atomic structure in thin films of silicon nitride and silicon diimide produced by remote plasma-enhanced chemical-vapor deposition," *Phys. Rev. B*, vol. 33, no. 10, pp. 7069-7076, 1986.
- [21] T. J. Cotler and J. Chapple-Sokol, "High quality plasma-enhanced chemical vapor deposited silicon nitride films," *J. Electrochem. Soc.*, vol. 140, pp. 2071-2075, 1993.
- [22] M. K. Mazumder, K. Kobayashi, J. Mitsuhashi, and H. Koyama, "Stress-induced current in nitride and oxidized nitride thin films," *IEEE Trans. Electron Devices*, vol. 41, pp. 2417-2422, Dec. 1994.
- [23] C.-L. Hwang, "High dielectric constant materials for ULSI applications," Ph.D. thesis, Yale Univ., New Haven, CT, pp. 31-44, 1994.
- [24] H. Tseng, "Application of JVD nitride gate dielectric to a 0.35 micron CMOS process for reduction of gate leakage current and boron penetration," in *IEDM Tech. Dig.*, Dec. 1997, pp. 647-650.
- [25] E. H. Nicollian and A. Goetzberger, "The Si-SiO<sub>2</sub> interface electrical properties as determined by the metal-insulator-silicon conductance technique," *Bell Syst. Tech. J.*, vol. 46, no. 6, pp. 1055-1133, 1967.
- [26] E. M. Vogel, W. L. Hill, V. Misra, P. K. McLarty, J. J. Wortman, J. R. Hauser, P. Morfouli, G. Ghigaud, and T. Ouisse, "Mobility behavior of n-channel and p-channel MOSFET's with pxynitride gate dielectrics formed by low-pressure rapid thermal chemical vapor deposition," *IEEE Trans. Electron Devices*, vol. 43, pp. 753-758, May 1996.
- [27] D. M. Fleetwood, "Border traps in MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 39, pp. 269-271, Feb. 1992.
- [28] H. C. Cheng, H. W. Liu, H. P. Su, and G. Hong, "Superior low-pressure-oxidized Si<sub>3</sub>N<sub>4</sub> films on rapid-thermal-nitrated poly-Si for high-density DRAM's," *IEEE Electron Device Lett.*, vol. 16, pp. 509-511, Nov. 1995.
- [29] K. Kobayashi, Y. Inaba, T. Ogata, T. Katayama, H. Watanabe, Y. Matsui, and M. Hirayama, "Ultrathin silicon nitride films fabricated by single-wafer processing using an SiH<sub>2</sub>Cl<sub>2</sub>-NH<sub>3</sub>-H<sub>2</sub> system and *in situ* H<sub>2</sub> cleaning," *J. Electrochem. Soc.*, vol. 143, pp. 1459-1464, 1996.

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