

## Features and Benefits of Silicon-on-Sapphire technology

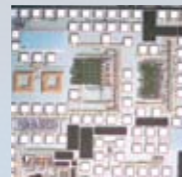
Transistors are placed in a thin layer of Silicon on an insulating substrate of Sapphire to provide a range of unique features that make it ideal for mixed signal applications.

Feature	Benefit
Little or no parasitic capacitance	Higher speeds and lower power consumption
Fully depleted transistors	Faster switching speeds and lower noise
Very high Fmax (100GHz on 0.25µm device)	Ideal for high frequency RF applications
Standard CMOS processing	Low cost with high performance
Integrated EEPROM with no extra masks	EEPROM works well – even at low voltages.
Very linear 3 terminal MOSFET devices (+38dBm IP3 mixers)	Excellent for demanding analog designs
High Q Inductors ( $Q_L > 40$ at 2GHz for 5 nH inductor)	Save cost + space by integrating passives on chip
Excellent thermal properties compared to bulk silicon	No self-heating problems - unlike other SOI technologies that use SiO2 as the insulator
Multiple threshold voltage options	Can mix high and low voltages on same chip

**For over 20 years the team at Sapphicon Semiconductor has been assisting customers to increase the performance and functionality of their products.**

Formerly a part of Peregrine Semiconductor the company now services a global client base as an independent organization with headquarters and manufacturing in Sydney, Australia.

The company uses advanced Silicon-on-Sapphire process technology that makes possible the creation of high performance mixed signal/analog devices such as RF switches, low noise amplifiers, high frequency VCOs and a myriad of other applications.



Photograph courtesy of Yale University.



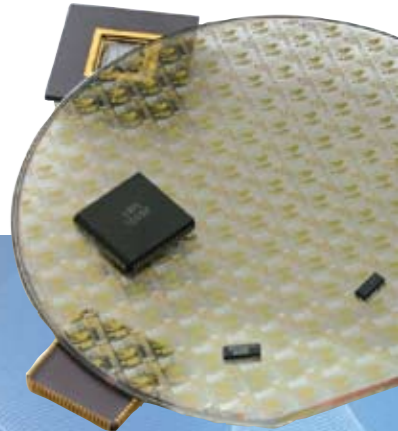
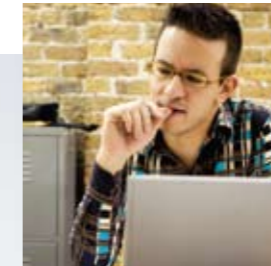
*Imagine the possibilities...*



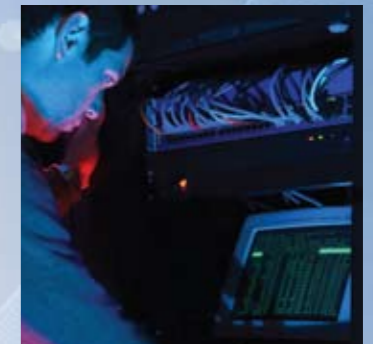
8 Herb Elliott Avenue, Homebush Sydney NSW 2127  
T + 612 9763 4111 F +612 9746 1501 sales@sapphicon.com www.sapphicon.com

# Compressed Reticle

*The next generation in low cost IC prototyping using Silicon-on-Sapphire*

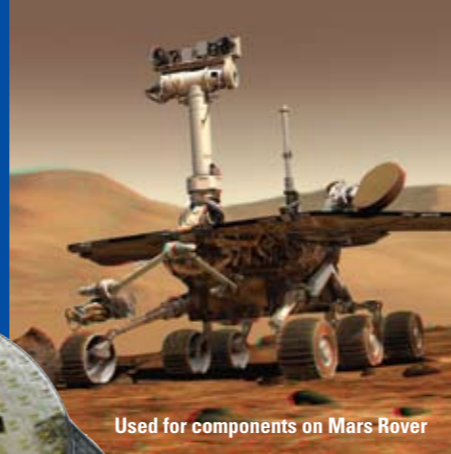
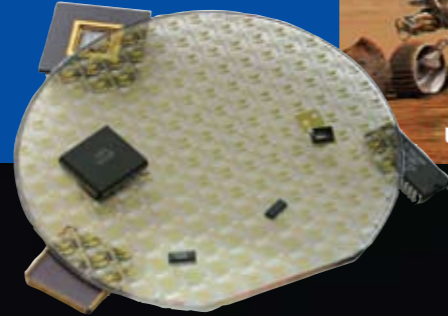


*Imagine the possibilities...*



# Compressed Reticle

Bring your chip design into reality with low cost prototyping service



Used for components on Mars Rover



Aerospace / Defence applications.



Square Kilometre Array Radio telescope



## 5 compelling reasons to use Compressed Reticles

### > Price

Compressed Reticle overcomes the prohibitive cost of mask tooling by arranging multiple images onto each photo mask thereby using only 2 or 3 masks instead of 15+ that are normally required.

### > Performance

Silicon-on-Sapphire process technology enables designs with lower power, higher frequency and lower noise specs compared to traditional bulk CMOS processes.

### > Personalized

The entire wafer is dedicated to your design, not shared with other customers.

### > Priority

Since the wafer is not shared with others, processing can begin when you are ready. There are no hard tape-out deadlines.

### > Production

In many instances the quantity of devices supplied is sufficient for an initial production run or will totally fulfil the low volume demand. For example, an initial production run may yield 500 - 10,000 chips depending on chip size.

**Silicon-on-Sapphire technology is ideal for mixed signal, RF and a range of other applications**

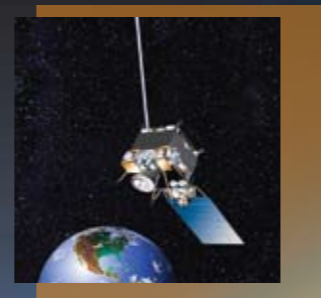
- > RF chips
- > Integrated analog, digital, passives (R,C,L) and RF
- > Very low noise amplifiers
- > High Speed, Low Jitter VCOs (e.g. >10GHz)
- > Low power, low voltage mixed signal chips
- > High power MOSFETs
- > Combined high and low power
- > MEMs
- > Photonics (Sapphire is optically clear)

### Sapphicon provides:

- > Custom chip design services;
- > Low cost prototyping services
- > Standard products based on Silicon-on-Sapphire technologies.



Photograph courtesy of Johns Hopkins University.



Space and radiation hard applications

Research Projects

Aerospace and Defence

Wireless Communication

Medical Applications

New Product Development

## Compressed Reticle is suitable for:

- > Universities
- > Research Institutions
- > Defence and Aerospace companies
- > Low volume applications
- > Producing trial samples prior to high volume ramp-up

## Compressed Reticle Specifications

Process Technologies	0.5µm or 0.25µm Silicon-on-Sapphire
Wafer size	150mm
Max Product Field Size	6.04 x 3.74 mm Area = 22.59 mm <sup>2</sup>
Approx. Fields per wafer	450

## Creating a design using Compressed Reticle prototyping

- > Sapphicon provides a process design kit for the SoS process.
- > Customer carries out the chip designs or uses Sapphicon supplied design services.
- > GDSII layout data is supplied to Sapphicon for final design rule checking and mask fabrication.
- > Sapphicon prepares mask data & sources the mask tooling.
- > Typically, two wafers are produced but additional wafers can be purchased.
- > Untested devices are supplied either as complete unsawn, wafers or packaged in a variety of prototype packages.



Typical Compressed Reticle: multiple photo-layers on each mask

